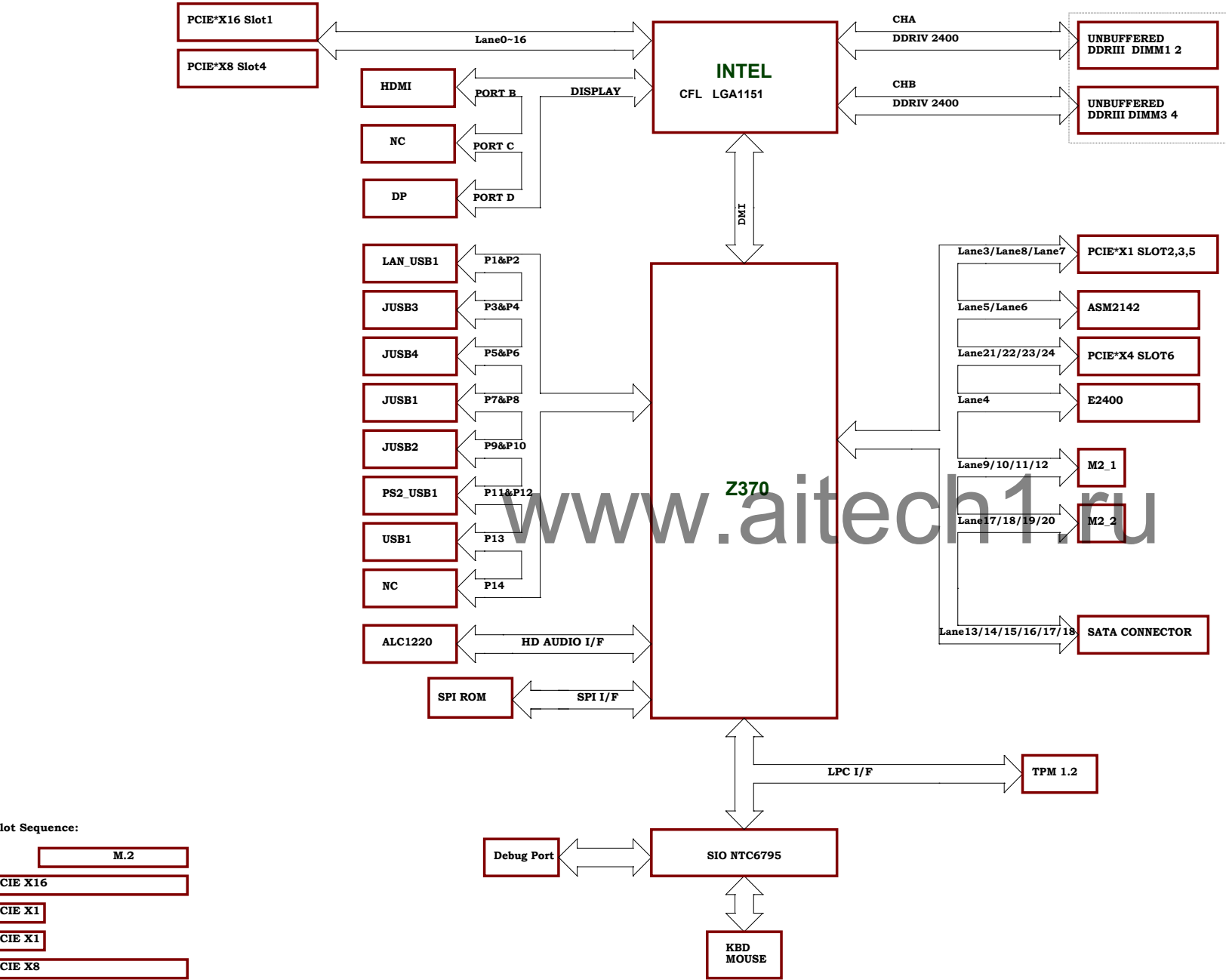
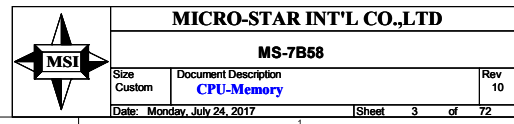
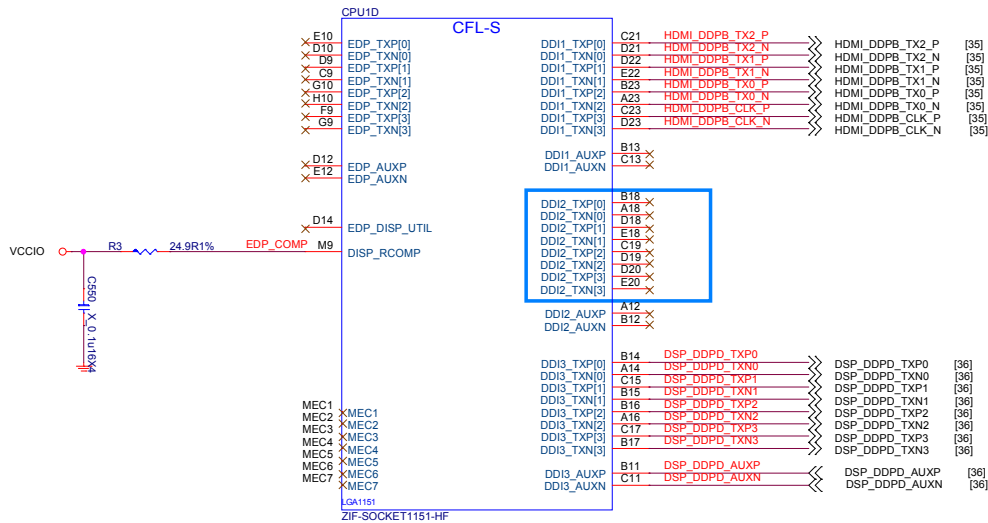
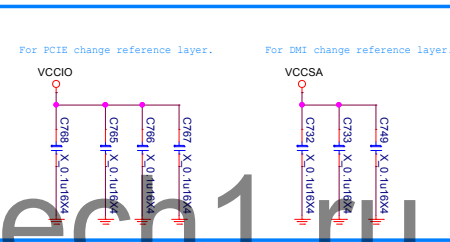
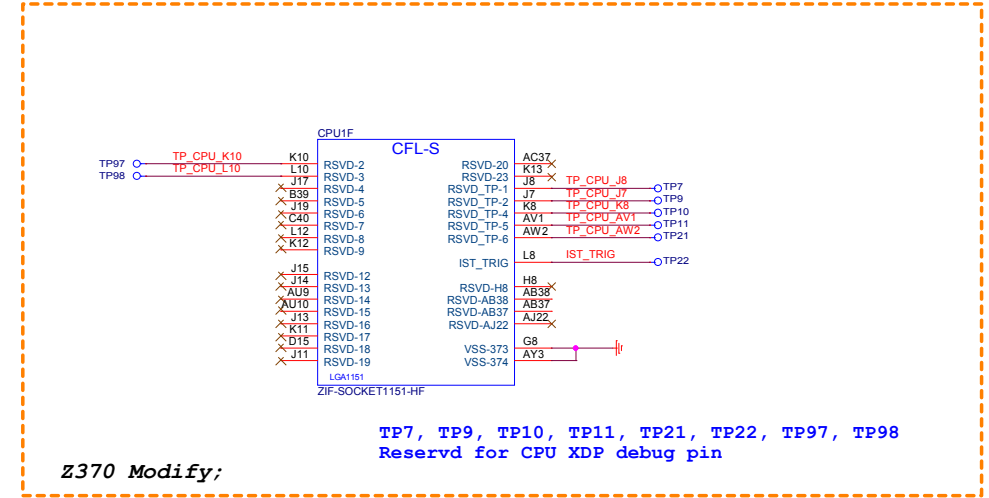
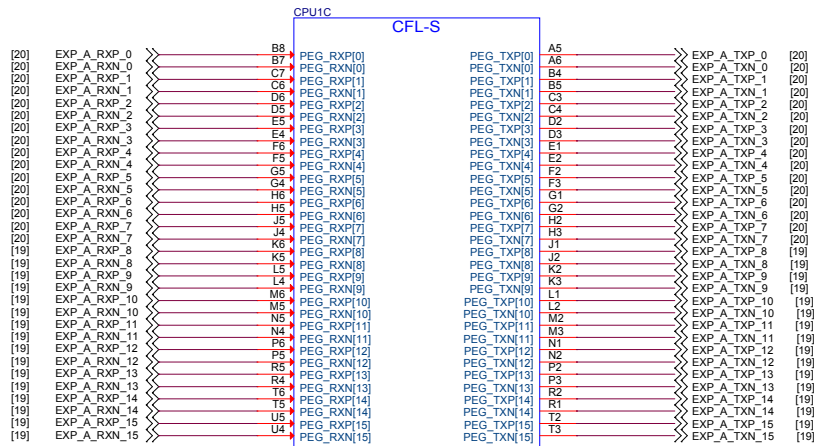
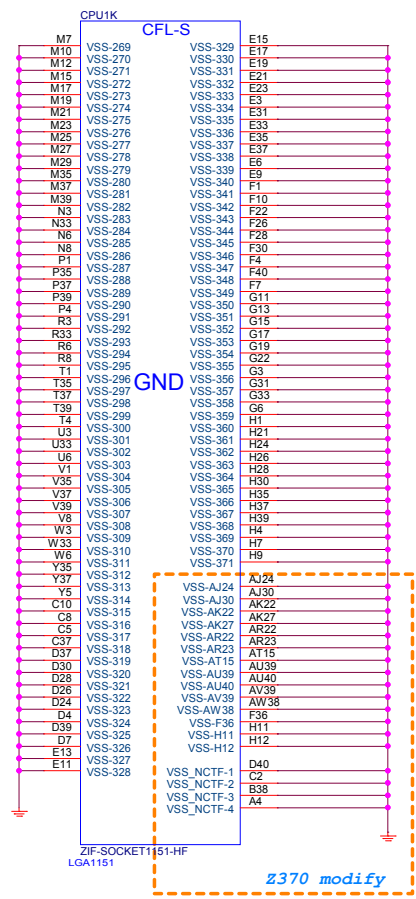
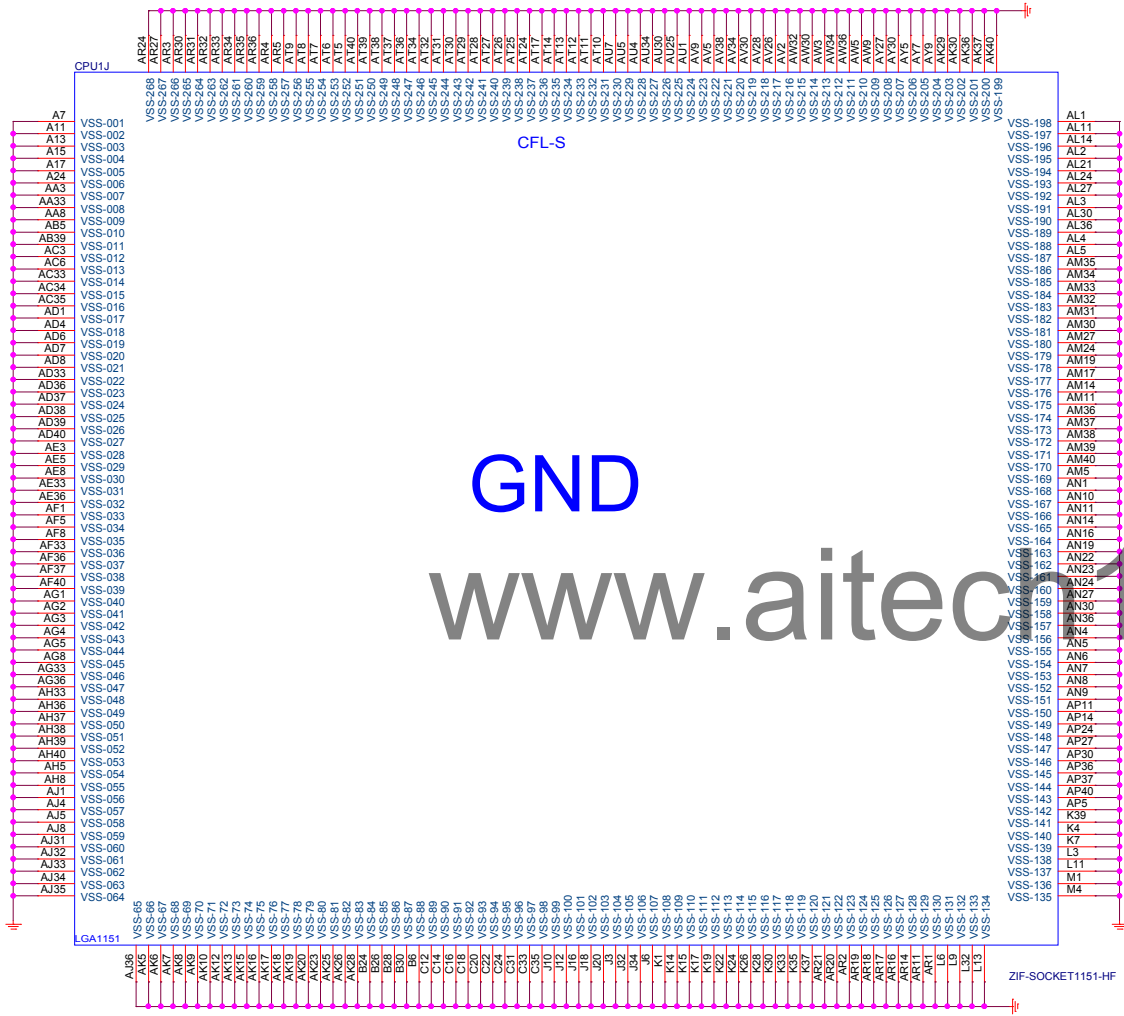


MS-7A78 Block Diagram



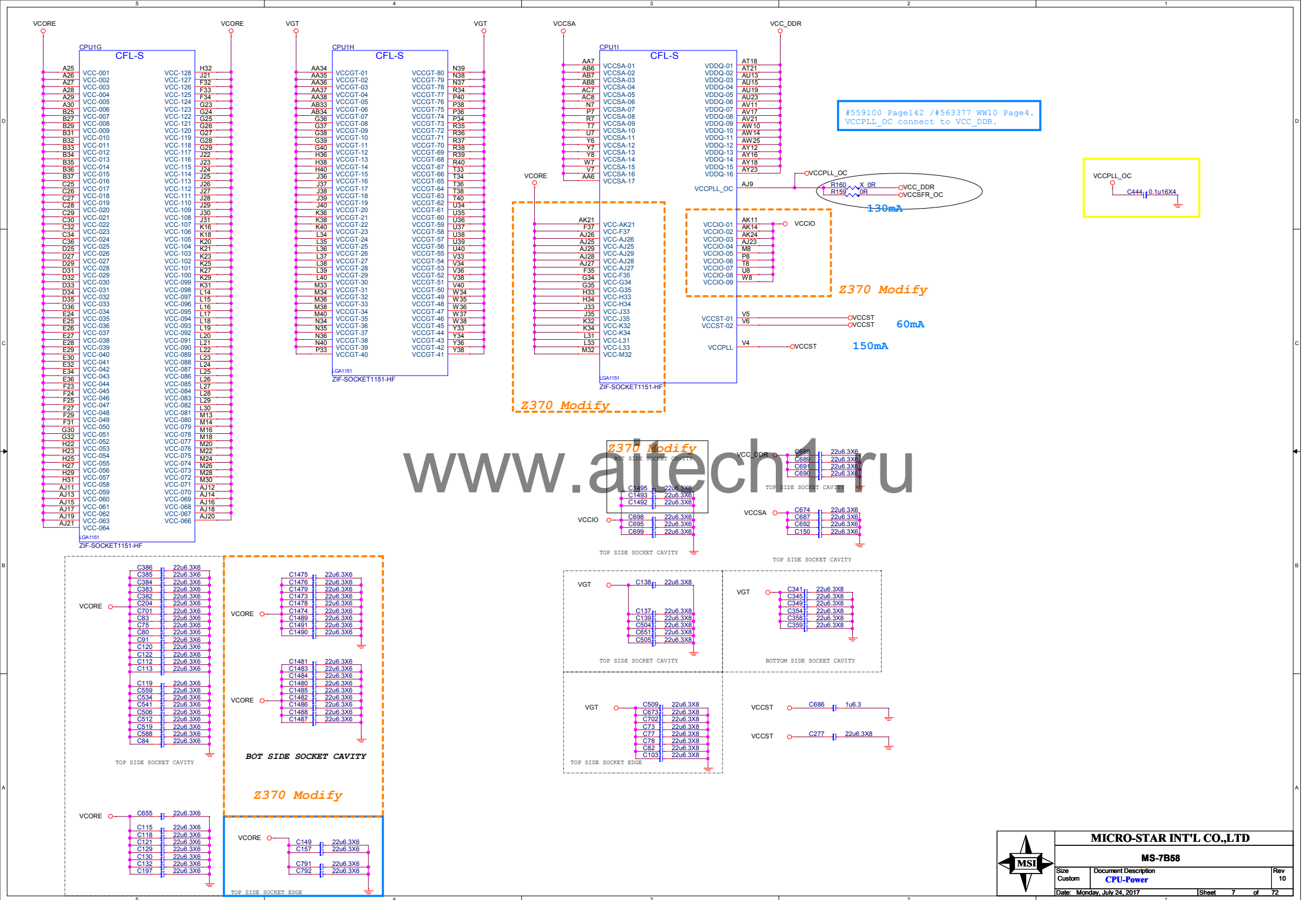






www.aitec1.ru

www.vinafix.com



MICRO-STAR INT'L CO.,LTD

MS-7B58

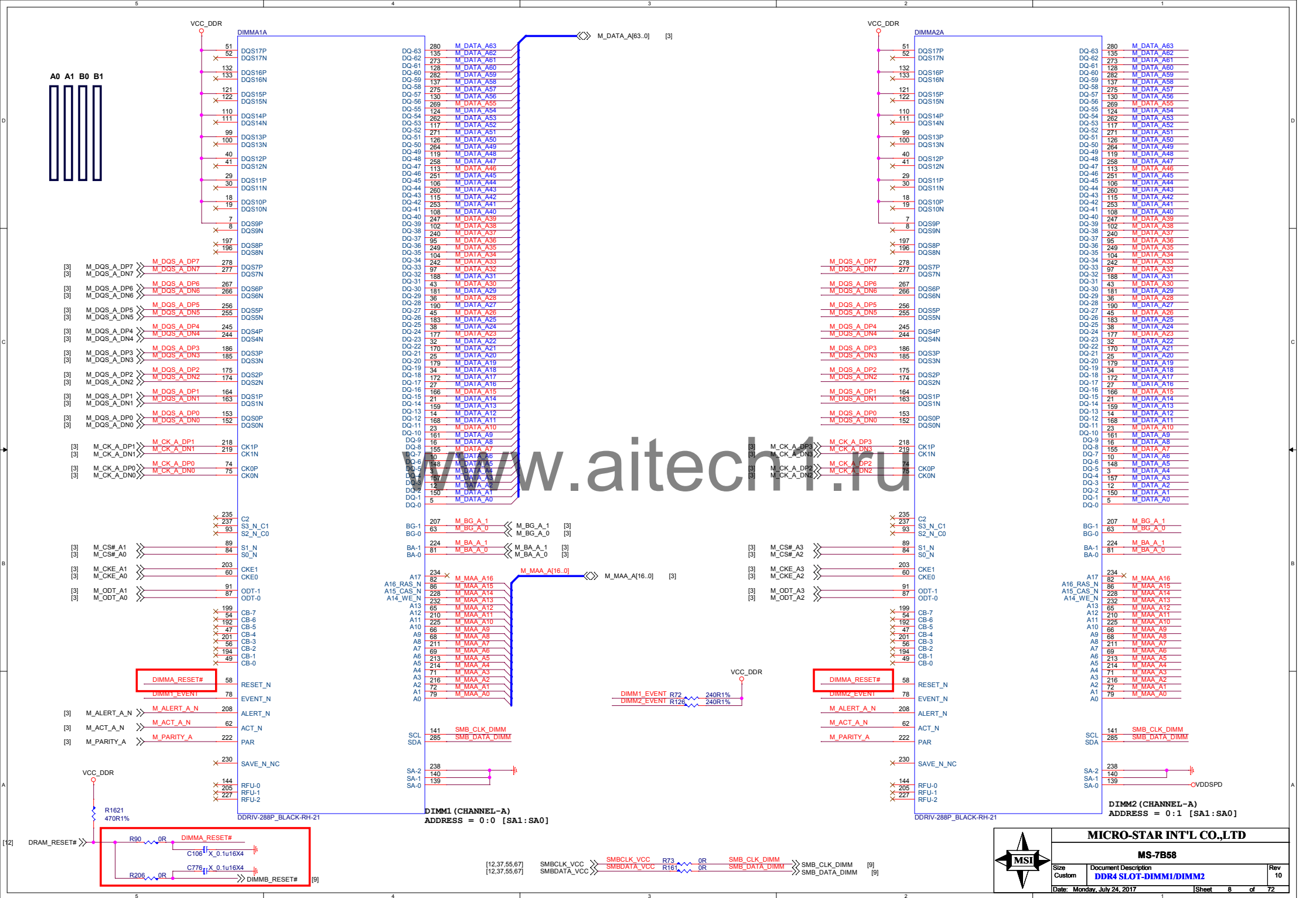
Size
Custom

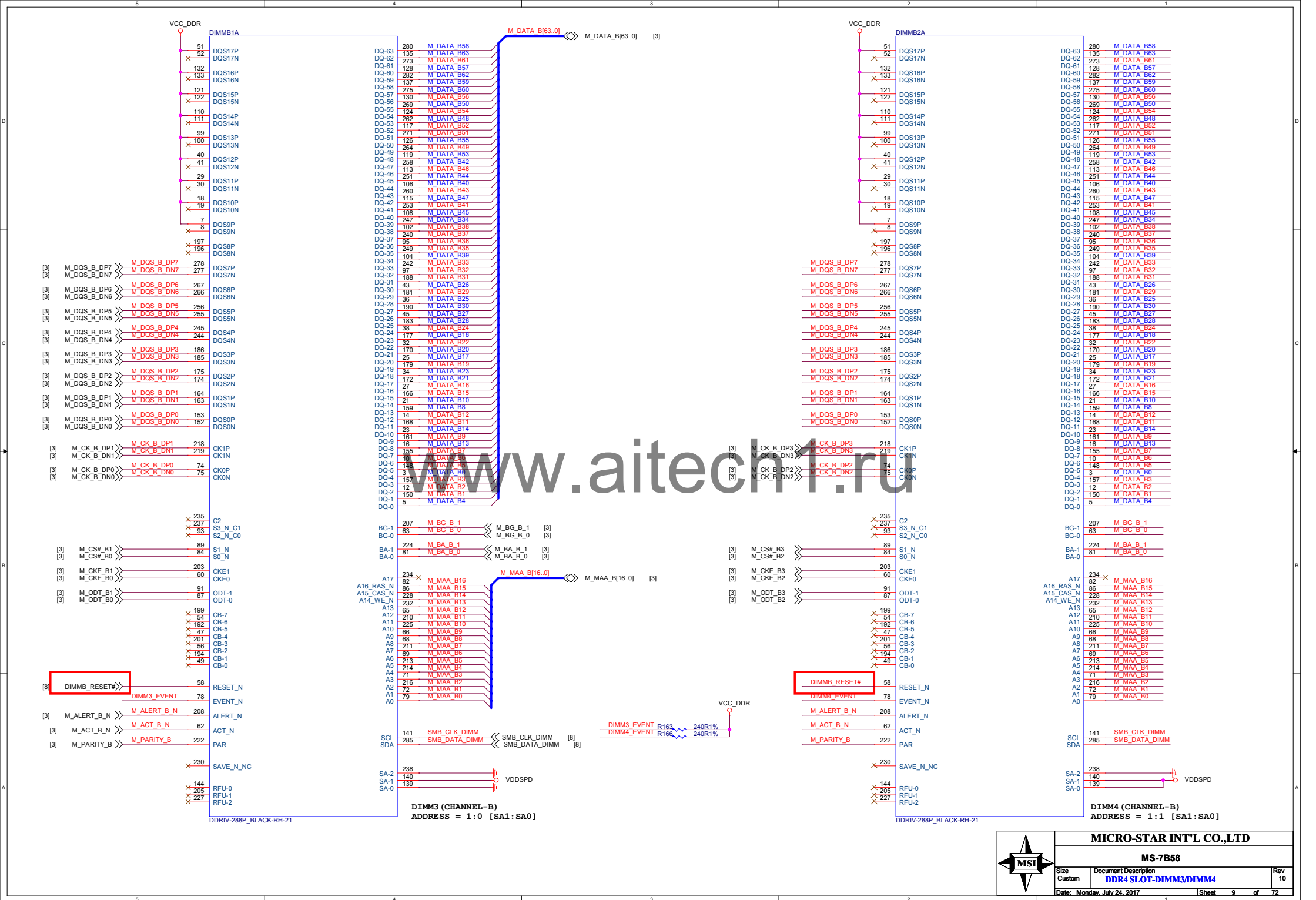
Document Description
CPU-Power

Rev	
10	

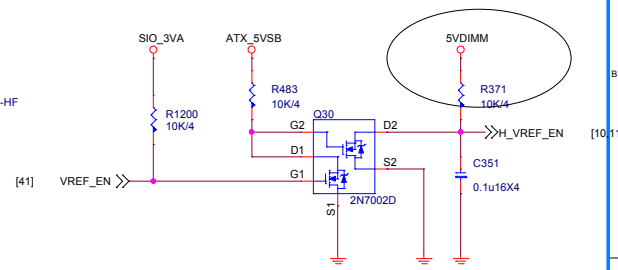
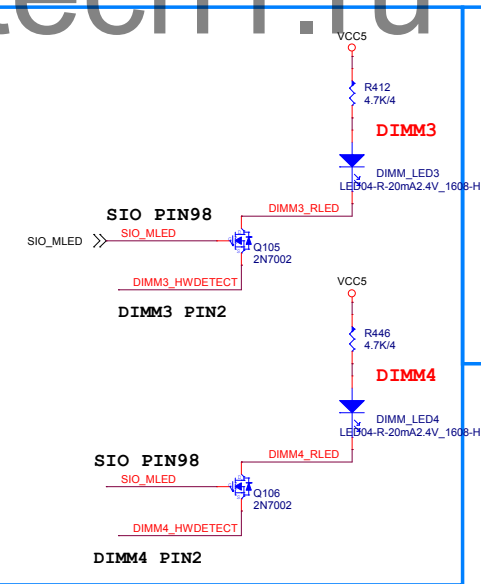
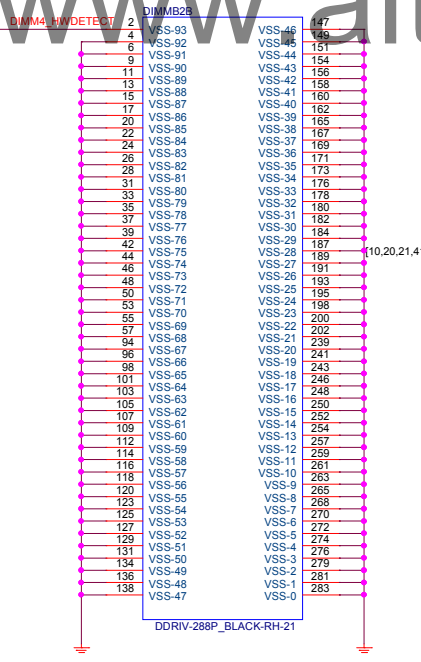
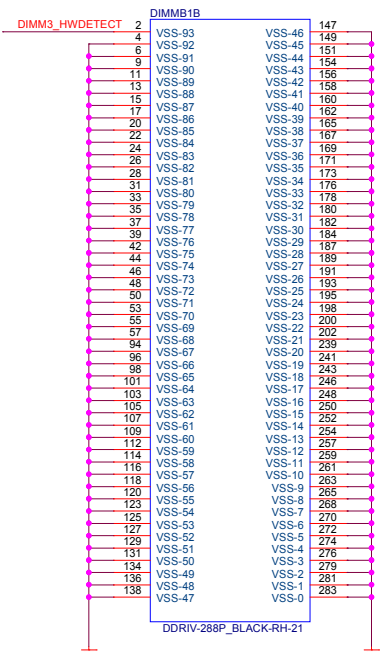
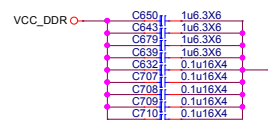
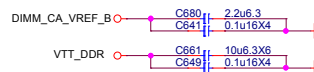
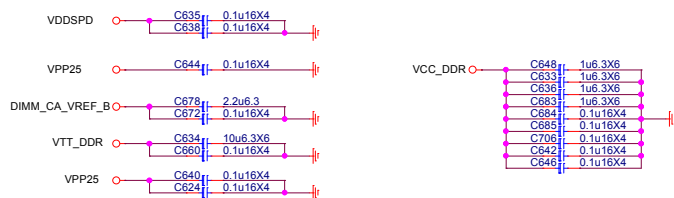
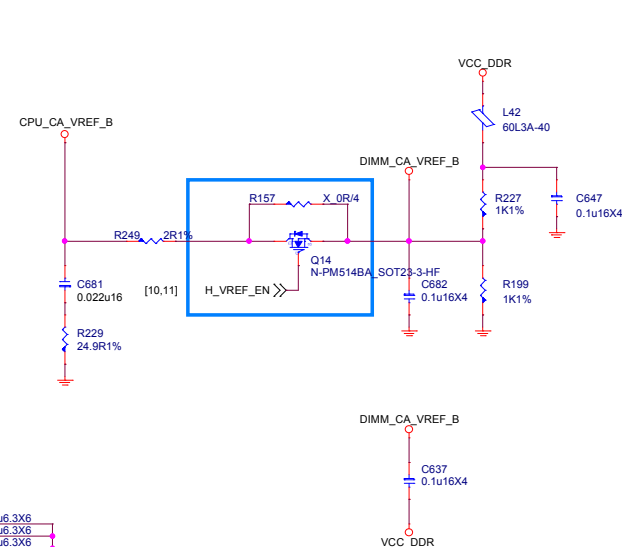
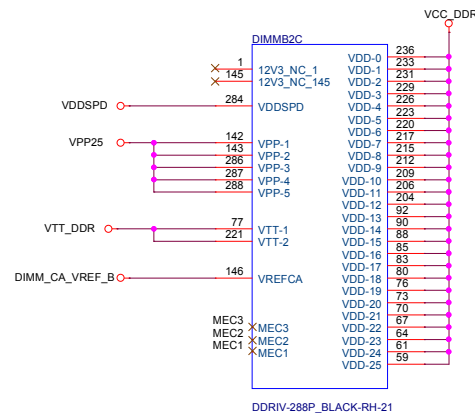
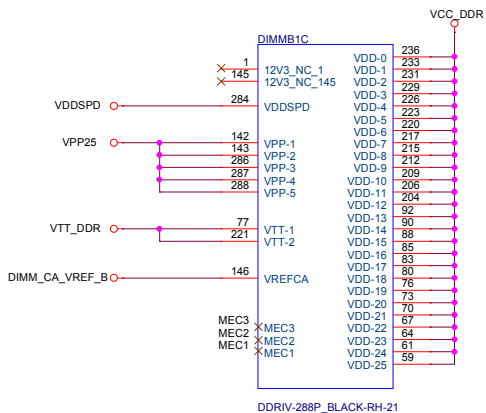
Date: Monday, July 24, 2017

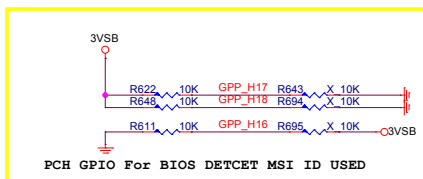
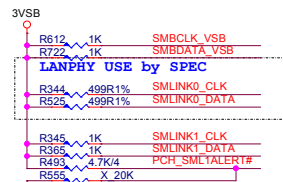
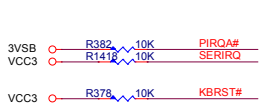
Sheet	7	of	72
-------	---	----	----



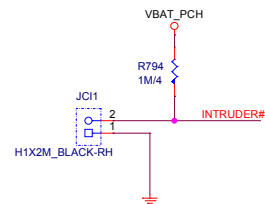




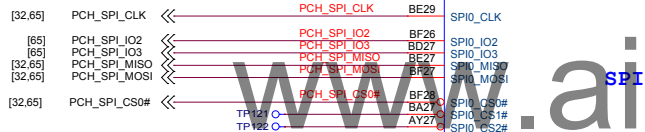
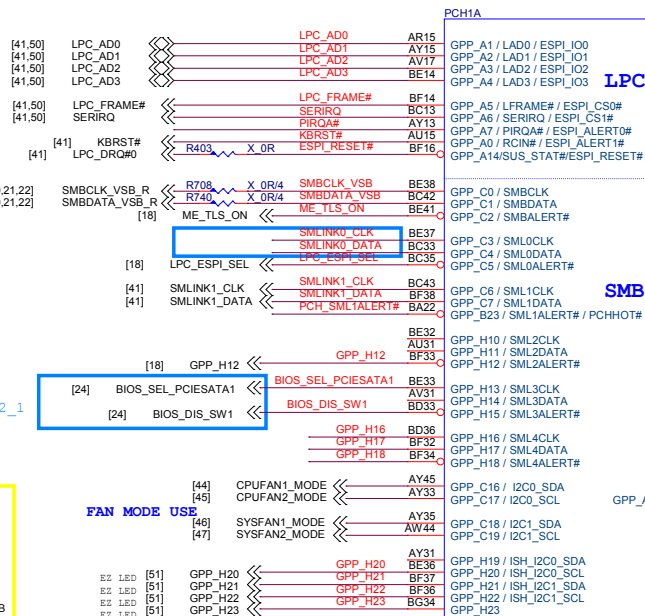
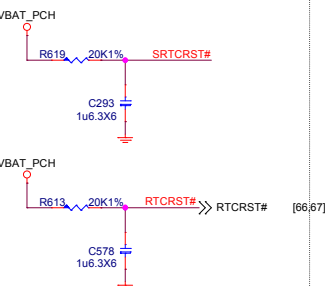




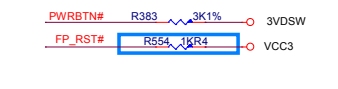
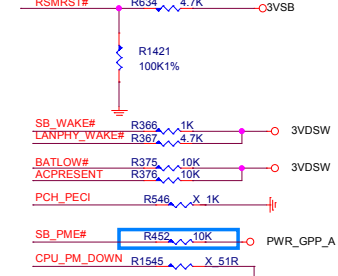
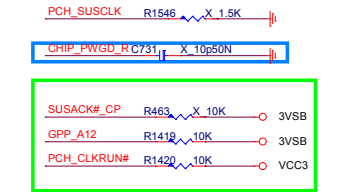
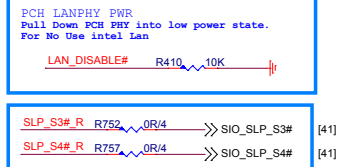
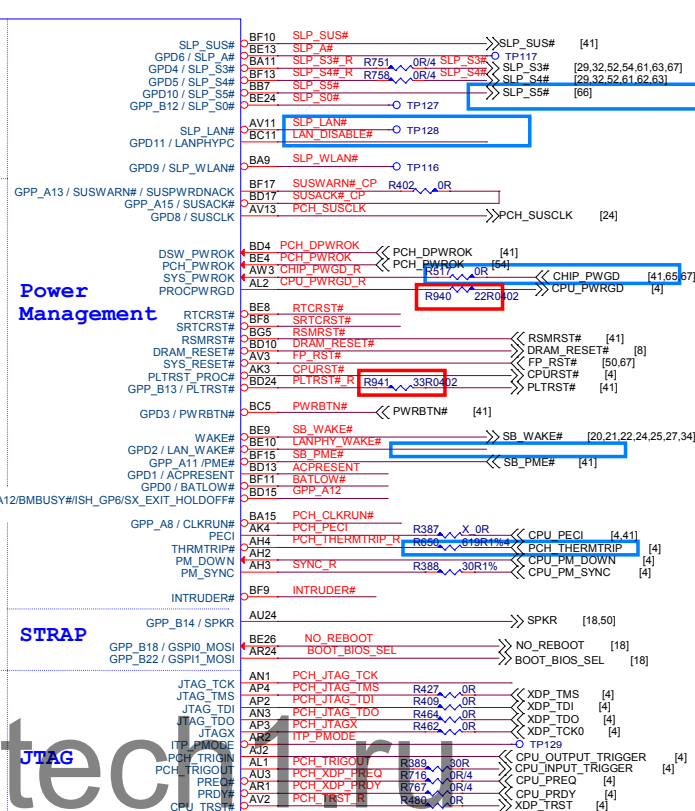
Chassis Intrusion



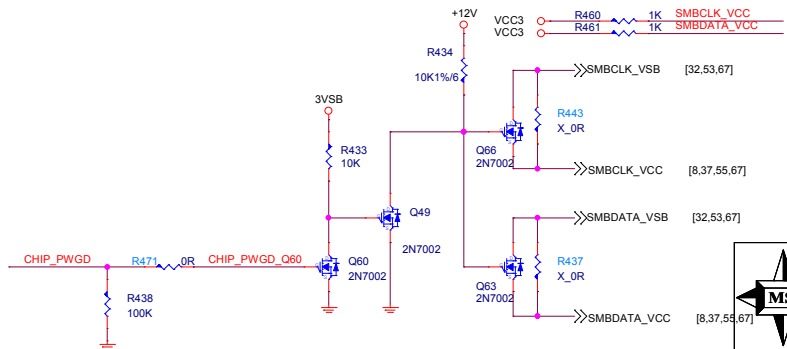
RTC



PCH1 change to OB1-7A58002-I06.



擺在一起 (注意到所有的SMBUS的分枝)

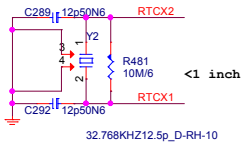


MICRO-STAR INT'L CO.,LTD		
MS-7B58		
Size	Document Description	Rev
Custom	PCH-Audio/Display/Clock	10
Date:	Monday, July 24, 2017	Sheet 12 of 72

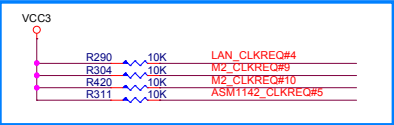
PCH_CLK

RTC Block

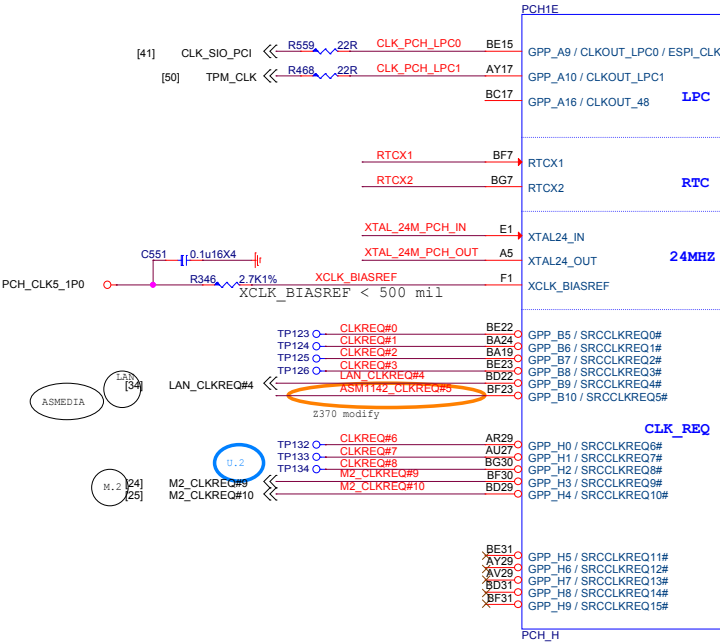
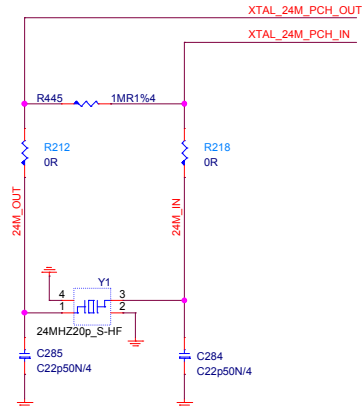
Close to PCH



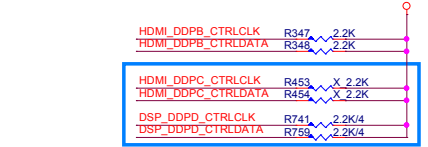
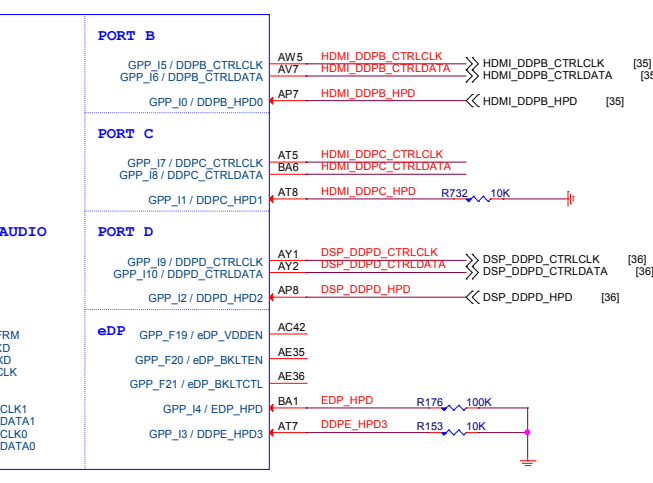
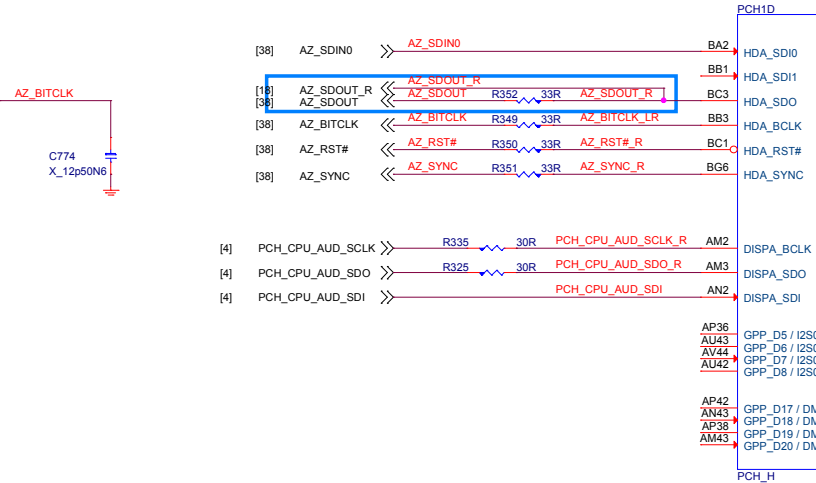
CRB
SRCCLKREQ pull up power change to VCC3.

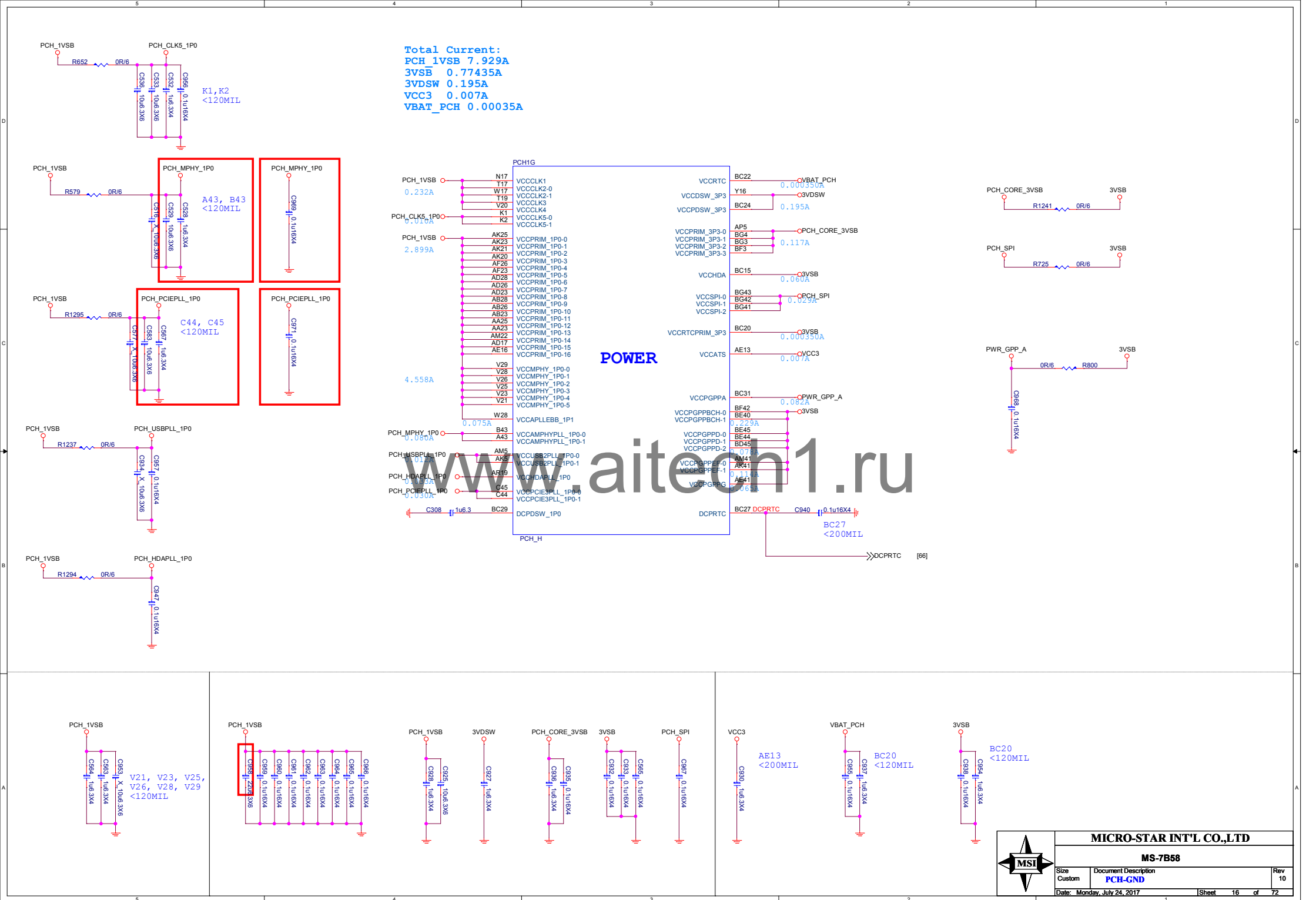


AVL: D04-0306001-C11/D04-0306101-T02



www.aitech1.ru





MICRO-STAR INT'L CO.,LTD

MS-7B58

Size
Custom

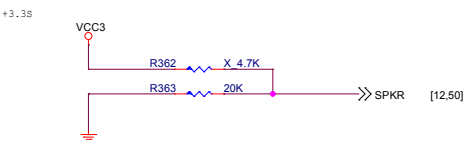
Document Description
PCH-GND

Rev	
10	

Date: Monday, July 24, 2017

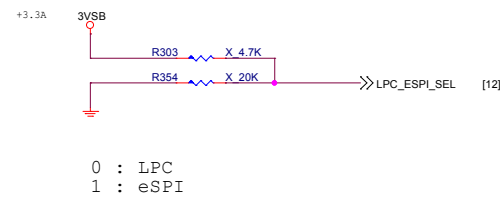
Sheet	16	of	72
-------	----	----	----

TOP Swap



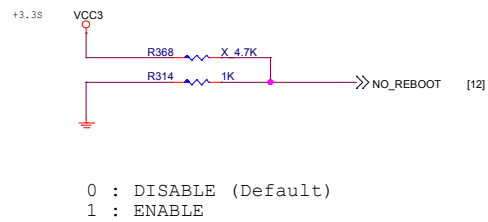
Internal pull-down is disabled after PLTRST#

LPC eSPI Mode



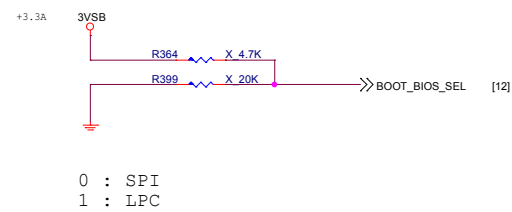
Internal pull-down is disabled after RSMRST

No Reboot



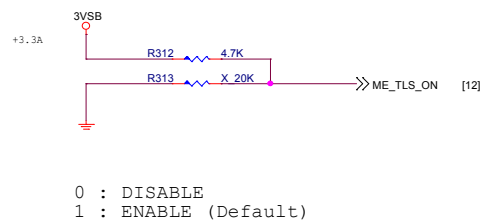
Internal pull-down is disabled after PLTRST#

Boot BIOS



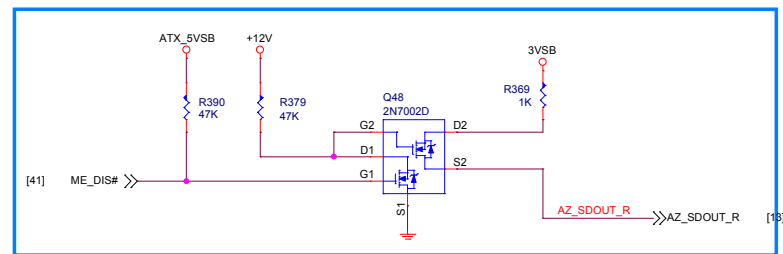
Internal pull-down is disabled after PLTRST

AMT and SBA with confidentiality

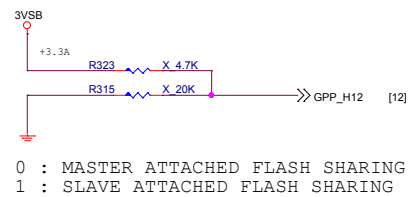


Internal pull-down is disabled after RSMRST

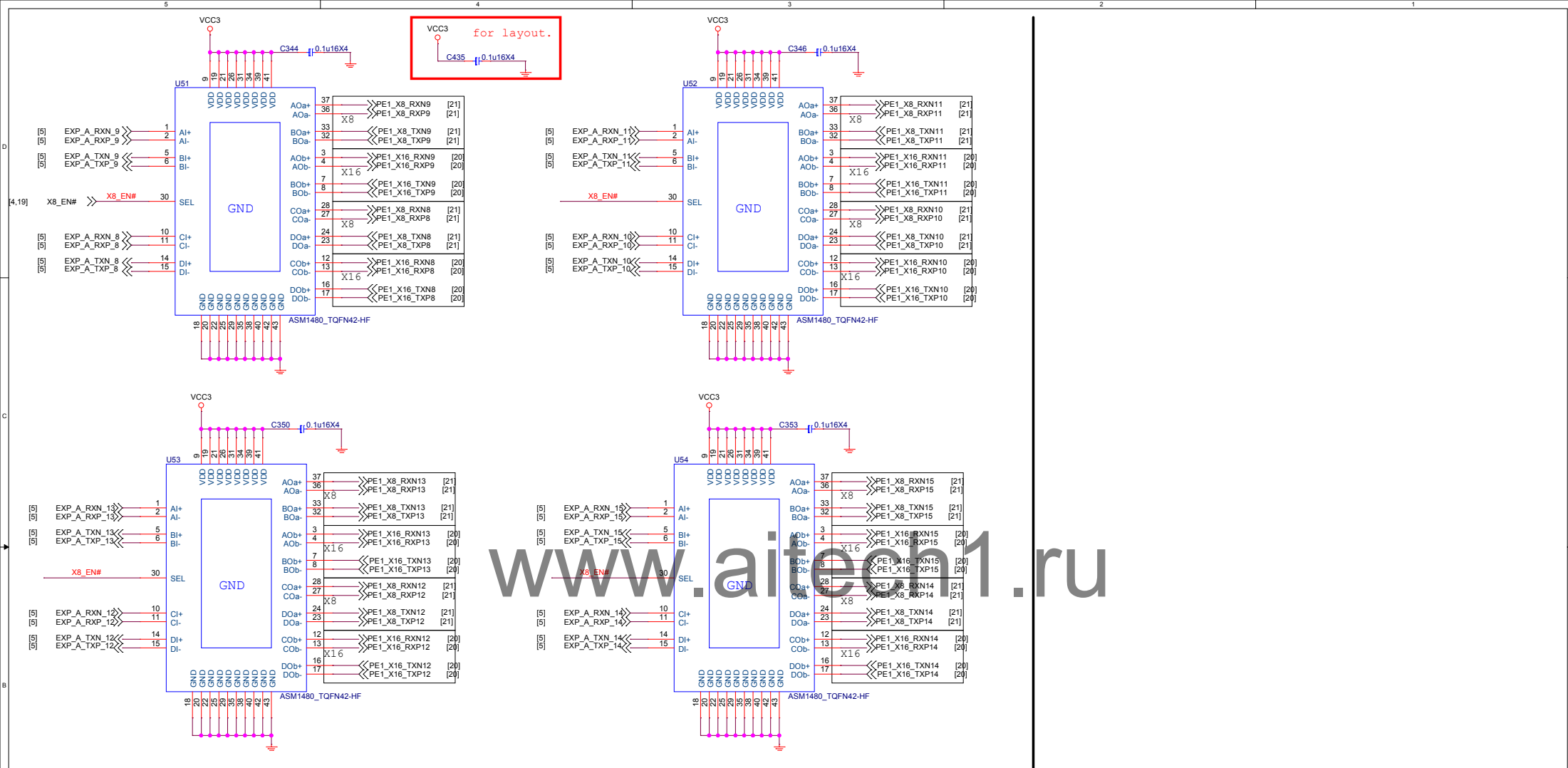
HDA_SDO



ESPI FLASH SHARING MODE



Internal pull-down is disabled after RSMRST



If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_1/3	
	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

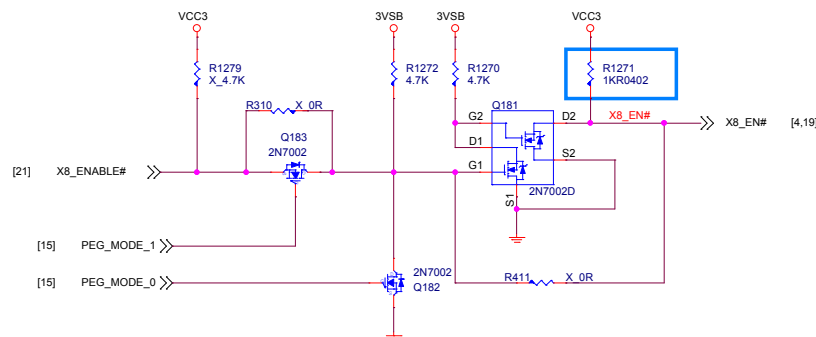
PCH Status	MODE_1	
	MODE_0	MODE_1
AUTO	0	1

MODE_1/3

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_1/3	
	MODE_0/2	MODE_1
AUTO	0	1



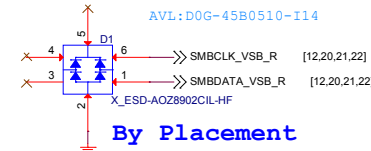
MICRO-STAR INT'L CO.,LTD		
MS-7B58		
Size Custom	Document Description PCI SWITCH	Rev 10
Date: Monday, July 24, 2017	Sheet 19 of 72	

P/N:W11-1641491-L06
Footprint:SLOT_PCIEXP164_13

12V - 5.5A
VCC3 - 3A
3VSB - 375mA

SMBCLK_VSB_R R676 4.7K/4
SMBDATA_VSB_R R681 4.7K/4

SMBUS ESD



GPIO LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

PCIE SLOT LED

PCH_GPP_C8

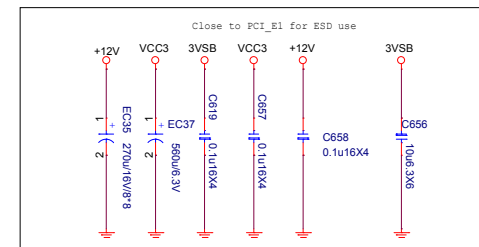
[15] PCIE2_16_EN >>

[15] PCIE2_8_EN >>

PCH_GPP_C9

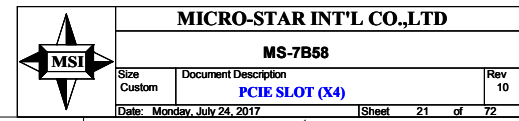
SIO_PIN98

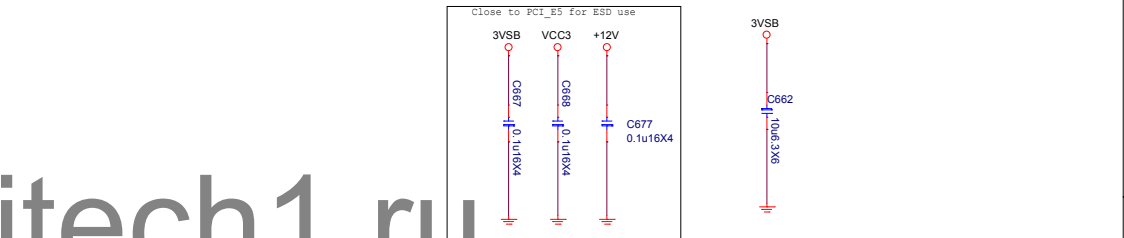
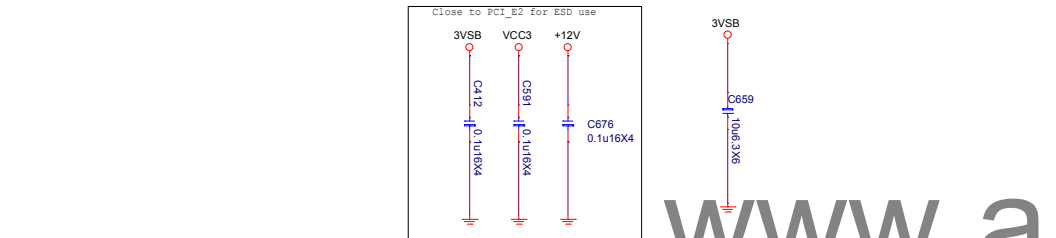
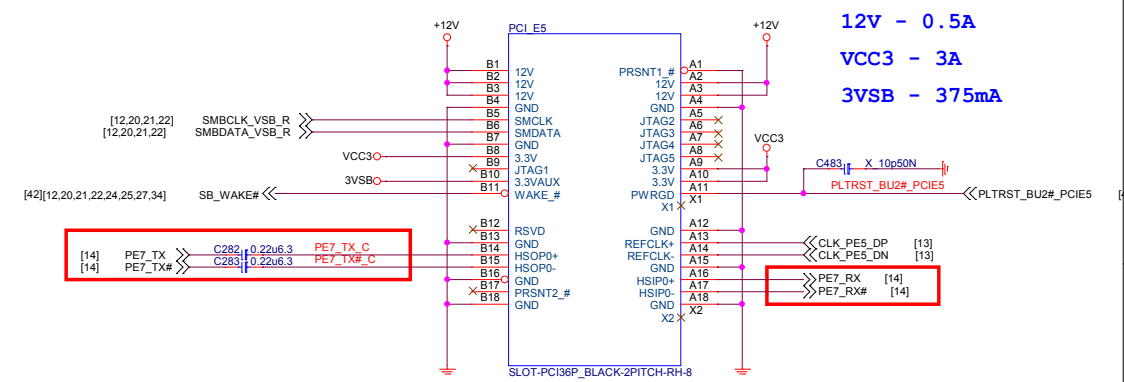
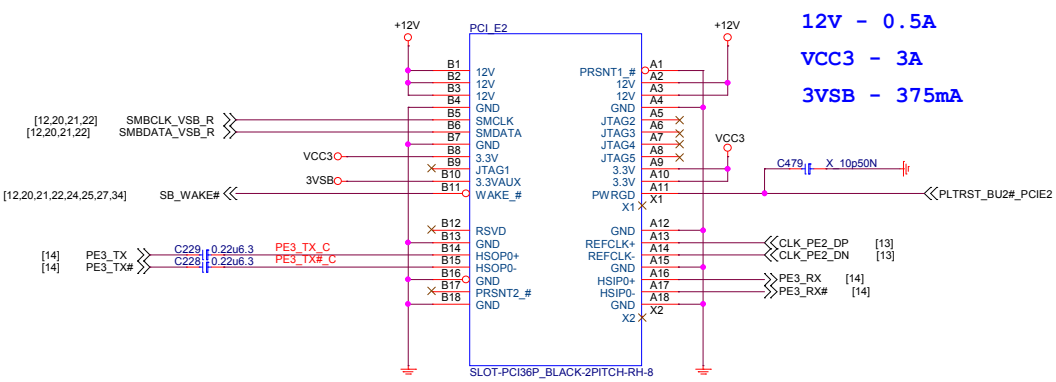
[10,11,21,41] SIO_MLED >>



12V - 2.1A
VCC3 - 3A
3VSB- 375mA

P/N:N11-1000151-L06
Footprint:SLOT_PCIEXP100_3

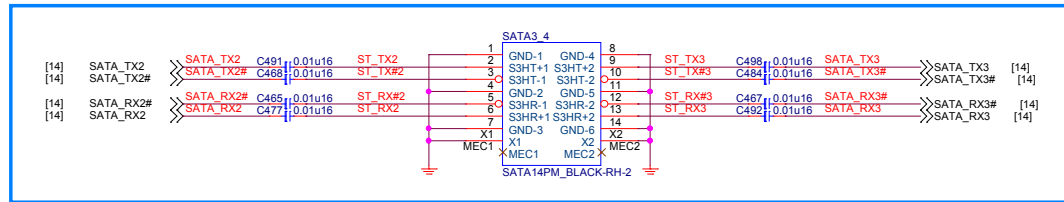
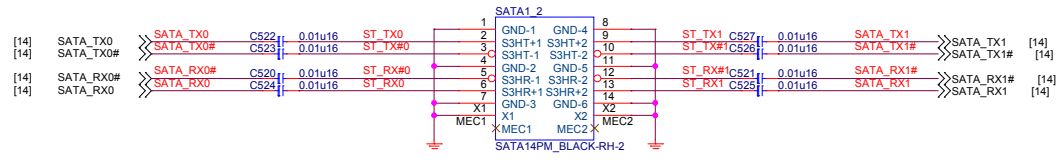




www.aitech1.ru

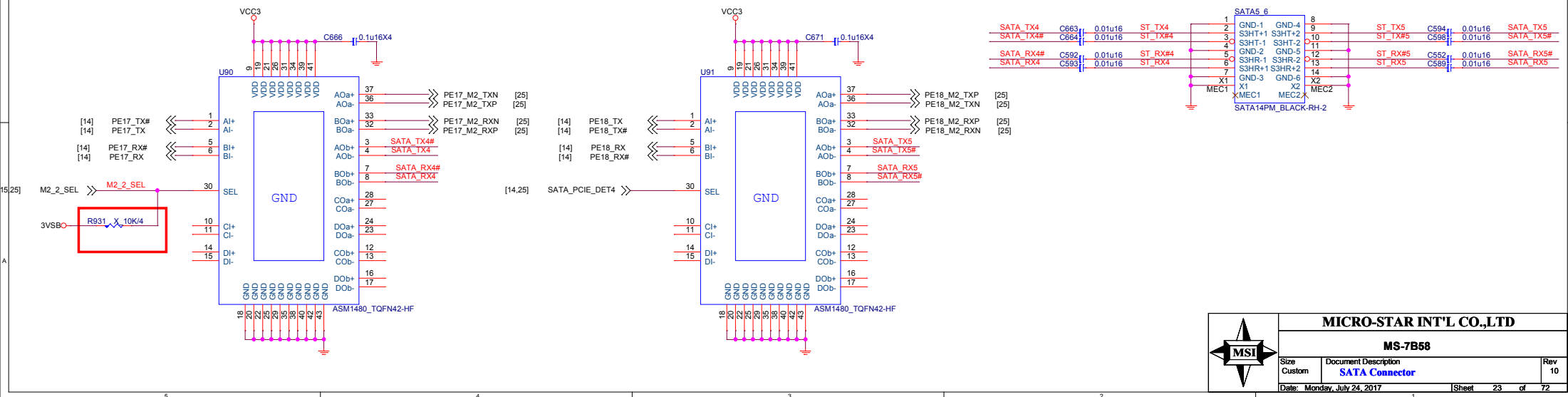


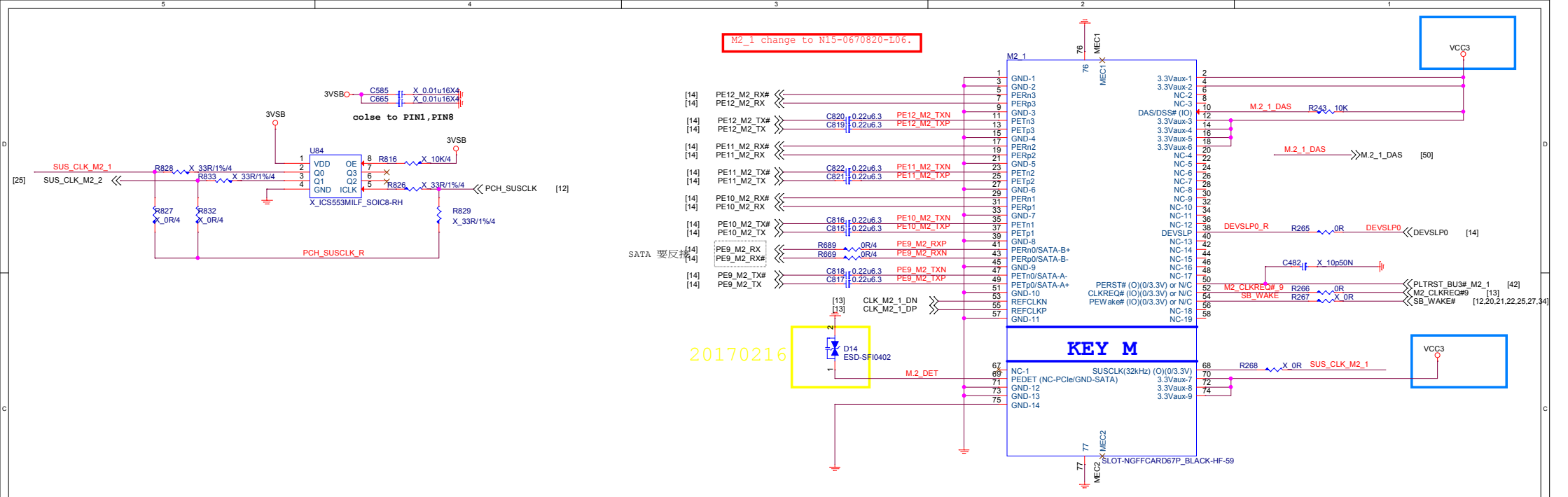
MICRO-STAR INT'L CO.,LTD		
MS-7B58		
Size Custom	Document Description	Rev 10
PCIE SLOT (X1)		
Date: Monday, July 24, 2017	Sheet 22	of 72



www.aitech1.ru

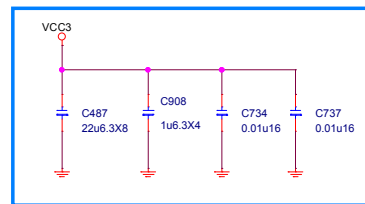
M2_2_SEL
0:to m2_2
1:to SATA



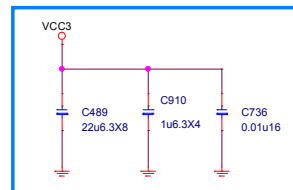


M.2 VCC3>=2.5A

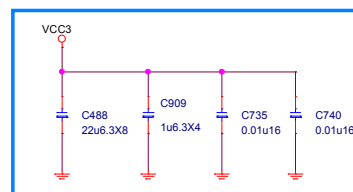
Near Pin2,Pin4



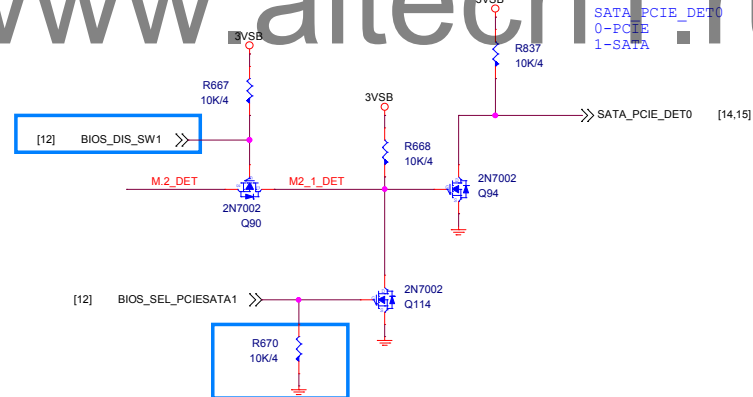
Near Pin12,Pin14,Pin16,Pin18



Near Pin70,Pin72,Pin74

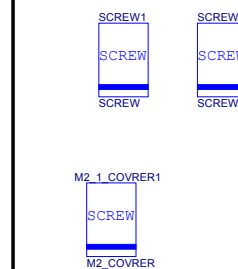
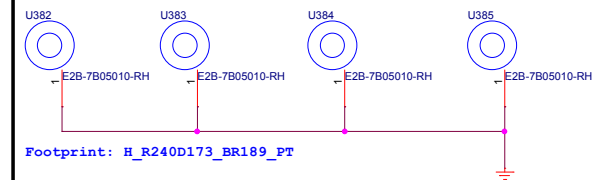


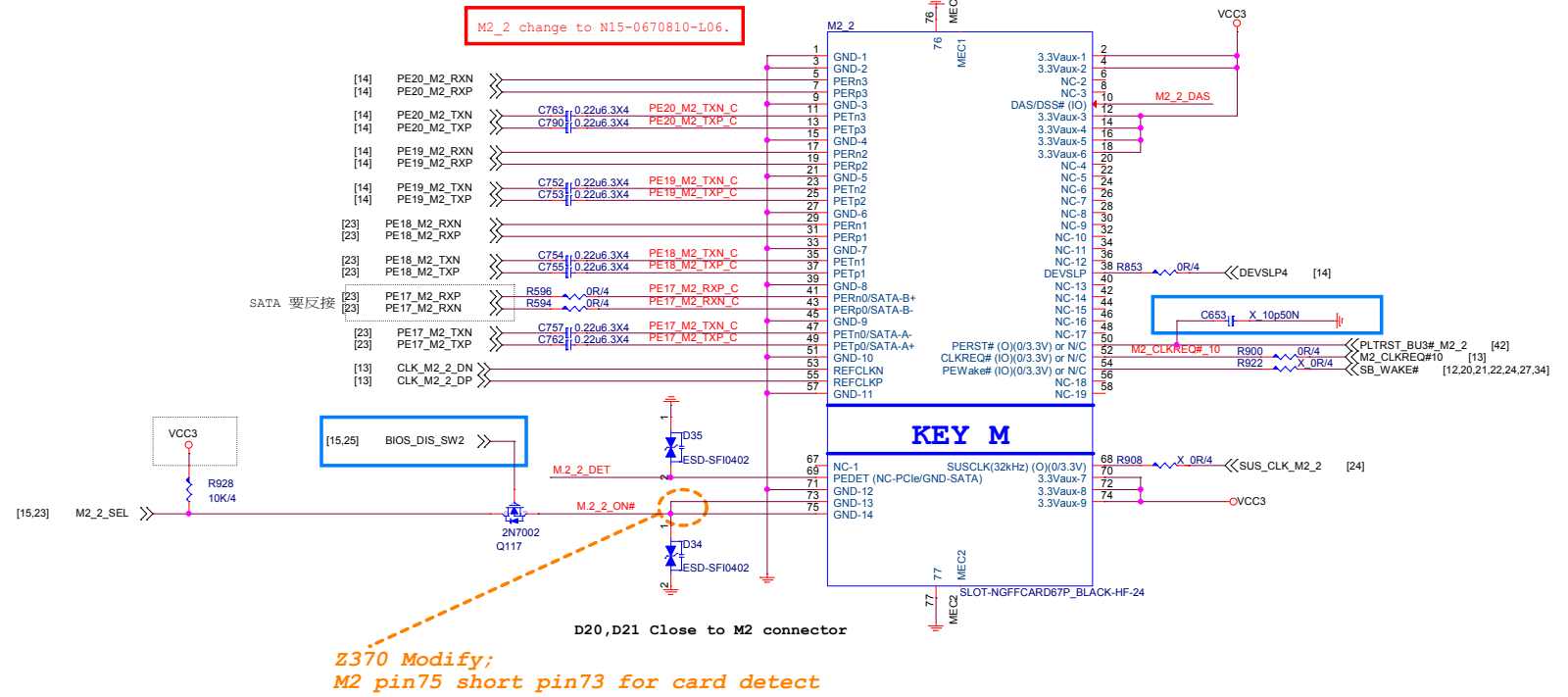
www.aitech1.ru



BIOS_MODE

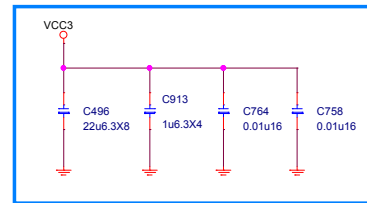
BIOS_DIS_SW	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIe
GPI	GPI	AUTO



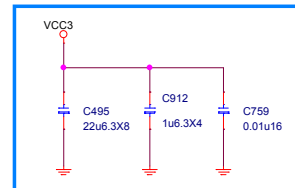


M.2 VCC3>=2.5A

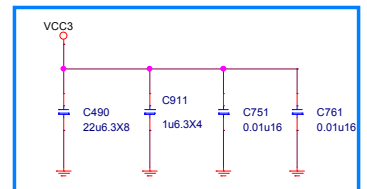
Near Pin2, Pin4



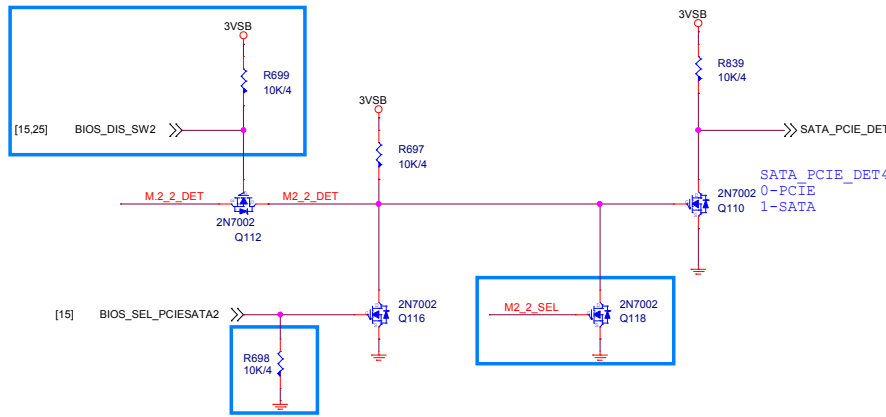
Near Pin12, Pin14, Pin16, Pin18



Near Pin70, Pin72, Pin74

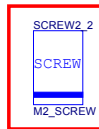
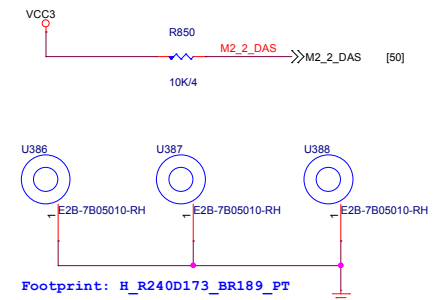


www.aitech1.ru




BIOS_MODE

BIOS_DIS_SW	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode
0	0	1	M2-SATA
0	0	0	M2-PCIE
GPI	GPI	GPI	AUTO



www.aitech1.ru

			MICRO-STAR INT'L CO.,LTD		
			MS-7B58		
Size	Document Description				Rev
Custom	U.2 Connector				10
Date: Monday, July 24, 2017			Sheet	26	of 72

Z370 modify ASM2142-->ASM3142

Minimum gap should be greater of >15mil with other signal.

CLK Rule (Follow SB PDG)

[13] CLK_ASM1142_DP
[13] CLK_ASM1142_DN

PE5_ASM_RX#
PE5_ASM_RX#
PE5_ASM_TX
PE5_ASM_TX#

PCIE Rule (Follow SB PDG)

PE6_ASM_RX
PE6_ASM_RX#
PE6_ASM_TX
PE6_ASM_TX#

C797 X 10p50N
PLTRST_BU1#_ASM1142
TPU1D

ASM_SMI1 2
SMI#
PORST#
USB_SPISCK
USB_SPISCB
USB_SPISI
USB_SPISCK

VCC3
RU17 80.6K1%
PONRST#
C99 1u16X4
RU20 4.7K
RU21 12.1K1%

SB_WAKE#
ASM1142_WAKE#
Q64 NN-2N7002D
S1 ASM_SMI1
3VSB 0.7K RU46
GPP_C23_USB3_SM1
VCC3 0.7K RU51

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

ASM3142

ASM3142-RH

P/N: B02-031420C-AD0

ASM3142 1.1v Core Power

ASM3142 2.5v Analog Power

ASM3142 1.1v Suspend Power

EEPROM

MS-M31-25L1022-M24 (1M)
S-M31-25X2023-W03 (2M)

MICRO-STAR INT'L CO.,LTD

MS-7B58

Size Custom
Document Description
ASM 1142
Date: Monday, July 24, 2017
Sheet 27 of 72

USB HS (90Ohm-Diff)

U2DP_A
U2DM_A

U3TXP_A
U3TXN_A
U3RXP_A
U3RXN_A

U2DP_B
U2DM_B

U3TXP_B
U3TXN_B
U3RXP_B
U3RXN_B

PRON_A
PRON_B

OCIA_A#
OCIB_A#

XI
XO

UART_RX
UART_TX

TEST_EN
REXT

ASM3142

ASM3142-RH

P/N: B02-031420C-AD0

ASM3142 1.1v Core Power

ASM3142 2.5v Analog Power

ASM3142 1.1v Suspend Power

EEPROM

MS-M31-25L1022-M24 (1M)
S-M31-25X2023-W03 (2M)

MICRO-STAR INT'L CO.,LTD

MS-7B58

Size Custom
Document Description
ASM 1142
Date: Monday, July 24, 2017
Sheet 27 of 72

Chip to Connector

SSD12+
SSD12-
SSD12+
SSD12-

SSTX12P
SSTX12N
SSRX12P
SSRX12N

SSD13+
SSD13-

SSTX13P
SSTX13N
SSRX13P
SSRX13N

PPONA
PPONB

OCIA
OCIB

XI
XO

UART_RX
UART_TX

TEST_EN
REXT

ASM3142

ASM3142-RH

P/N: B02-031420C-AD0

ASM3142 1.1v Core Power

ASM3142 2.5v Analog Power

ASM3142 1.1v Suspend Power

EEPROM

MS-M31-25L1022-M24 (1M)
S-M31-25X2023-W03 (2M)

MICRO-STAR INT'L CO.,LTD

MS-7B58

Size Custom
Document Description
ASM 1142
Date: Monday, July 24, 2017
Sheet 27 of 72

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"

2.) VIA hole < 2

For sata express mode use only.

X0/X1 (95hm-Diff, Spacing 30mil)
UREXT, PEUREXT(W/S): 10/7
OCIA, OCIB, PPONA, PPONB(W/S): 5/8

YU1
D04-0901200-F07
D04-0901100-T16

CU25 12p50N
YU1 20MHZ18p_S

CU21 0.1u16X4
CU22 0.1u16X4
CU23 0.1u16X4

CU24 0.1u16X4
CU25 0.1u16X4
CU26 0.1u16X4

CU27 0.1u16X4
CU28 0.1u16X4
CU29 0.1u16X4

CU30 0.1u16X4
CU31 0.1u16X4
CU32 0.1u16X4

CU33 0.1u16X4
CU34 0.1u16X4
CU35 0.1u16X4

CU36 0.1u16X4
CU37 0.1u16X4
CU38 0.1u16X4

CU39 0.1u16X4
CU40 0.1u16X4
CU41 0.1u16X4

CU42 0.1u16X4
CU43 0.1u16X4
CU44 0.1u16X4

CU45 0.1u16X4
CU46 0.1u16X4
CU47 0.1u16X4

CU48 0.1u16X4
CU49 0.1u16X4
CU50 0.1u16X4

CU51 0.1u16X4
CU52 0.1u16X4
CU53 0.1u16X4

CU54 0.1u16X4
CU55 0.1u16X4
CU56 0.1u16X4

CU57 0.1u16X4
CU58 0.1u16X4
CU59 0.1u16X4

CU60 0.1u16X4
CU61 0.1u16X4
CU62 0.1u16X4

ASM3142

NC-1
NC-2
NC-3
NC-4

VCCCH-1
VCCCH-2
VCCCLP-1
VCCCLP-2

VCCCHUS
VCCCHUS-1
VCCCHUS-2

VDD-1
VDD-2
VDD-3
VDD-4

VDDP-1
VDDP-2
VDDP-3
VDDP-4

VDDU-1
VDDU-2
VDDU-3
VDDU-4

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

ASM3142

NC-1
NC-2
NC-3
NC-4

VCCCH-1
VCCCH-2
VCCCLP-1
VCCCLP-2

VCCCHUS
VCCCHUS-1
VCCCHUS-2

VDD-1
VDD-2
VDD-3
VDD-4

VDDP-1
VDDP-2
VDDP-3
VDDP-4

VDDU-1
VDDU-2
VDDU-3
VDDU-4

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

ASM3142

NC-1
NC-2
NC-3
NC-4

VCCCH-1
VCCCH-2
VCCCLP-1
VCCCLP-2

VCCCHUS
VCCCHUS-1
VCCCHUS-2

VDD-1
VDD-2
VDD-3
VDD-4

VDDP-1
VDDP-2
VDDP-3
VDDP-4

VDDU-1
VDDU-2
VDDU-3
VDDU-4

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

ASM3142

NC-1
NC-2
NC-3
NC-4

VCCCH-1
VCCCH-2
VCCCLP-1
VCCCLP-2

VCCCHUS
VCCCHUS-1
VCCCHUS-2

VDD-1
VDD-2
VDD-3
VDD-4

VDDP-1
VDDP-2
VDDP-3
VDDP-4

VDDU-1
VDDU-2
VDDU-3
VDDU-4

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

ASM3142

NC-1
NC-2
NC-3
NC-4

VCCCH-1
VCCCH-2
VCCCLP-1
VCCCLP-2

VCCCHUS
VCCCHUS-1
VCCCHUS-2

VDD-1
VDD-2
VDD-3
VDD-4

VDDP-1
VDDP-2
VDDP-3
VDDP-4

VDDU-1
VDDU-2
VDDU-3
VDDU-4

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

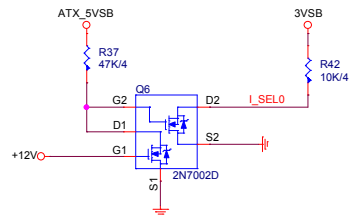
VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

VCC3
VCC3_2P5
VCC3_1P1
VCC3_1P1_VSB

Current Mode

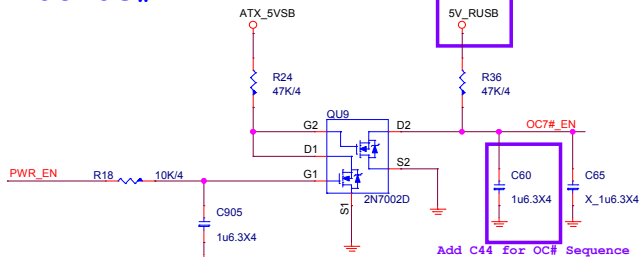


I_SELO: I_SEL1

X	0	1
I_SEL1	Default for 900mA	1.5A @5V
		3A @5V

1.5A under S3 mode
3A under S0 mode

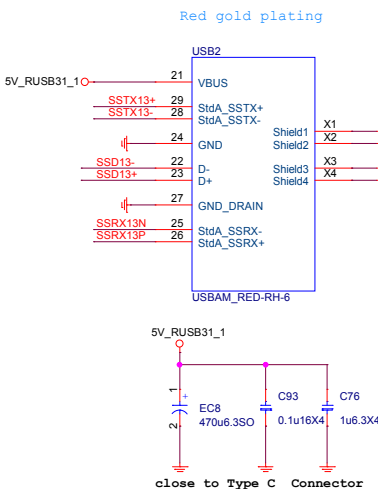
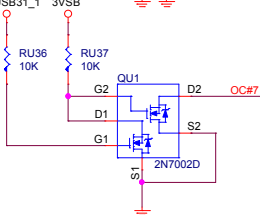
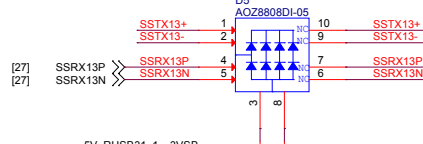
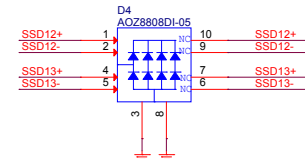
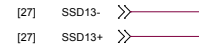
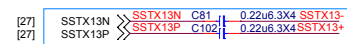
VBUS OC#



Add C44 for OC# Sequence

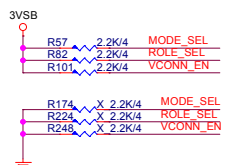
[14]

TYPE-A



close to Type C Connector

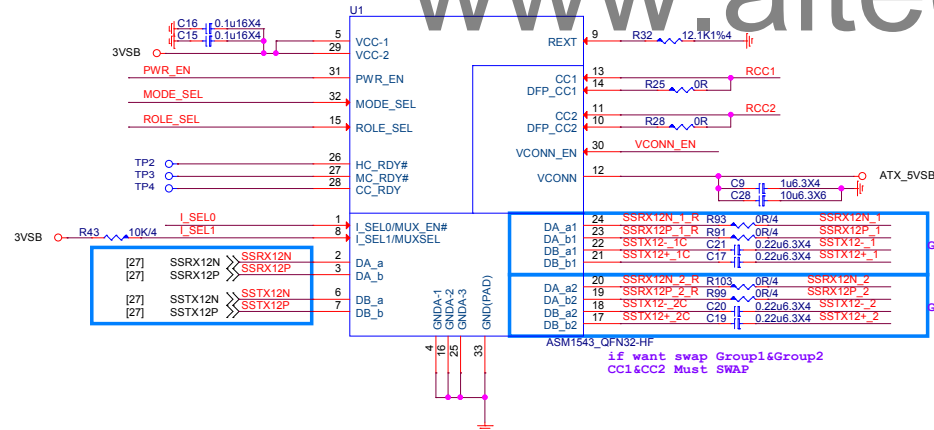
USB Type-C MUX with Configuration Channel (CC)



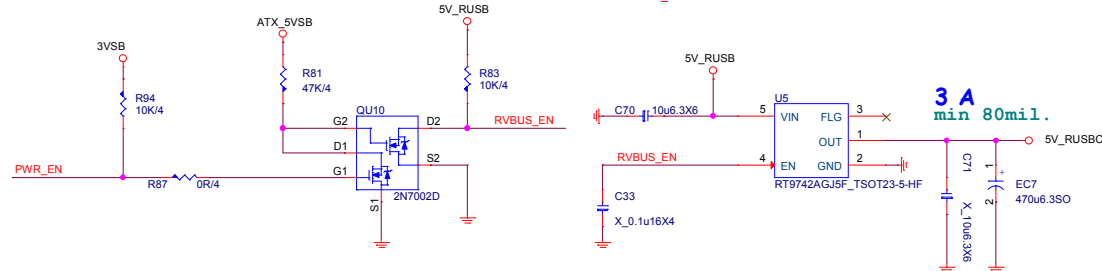
MODE_SEL
1
0

ROLE_SEL
1
0

VCONN_EN
1
0

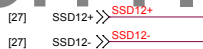


if want swap Group1&Group2
CC1&CC2 Must SWAP



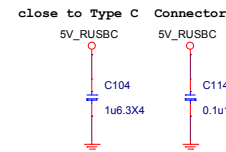
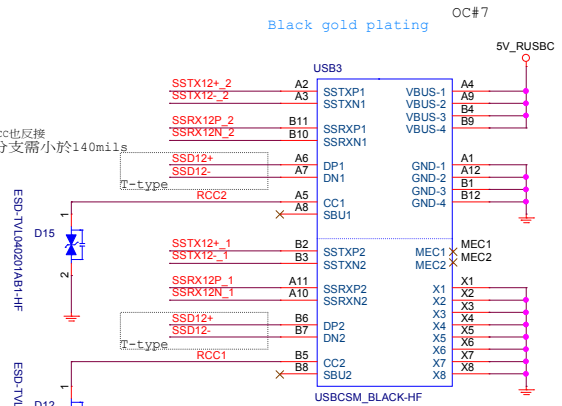
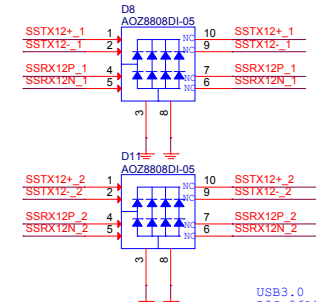
3 A
min 80mil.

TYPE-C



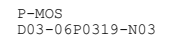
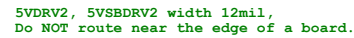
Port反結時CC也反接
T-type 分支需小於140mils

ESD Protection NEAR CONNECTOR



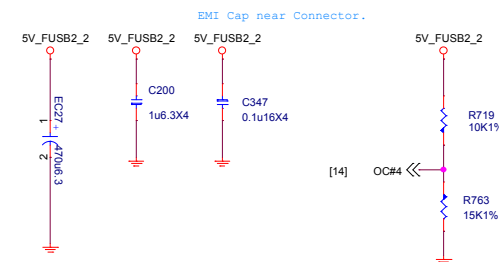
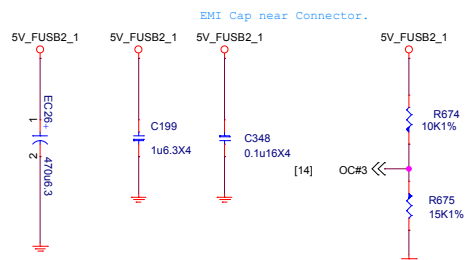
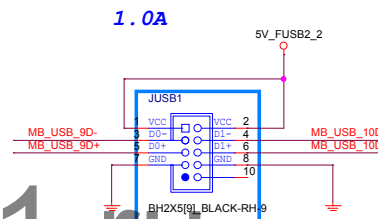
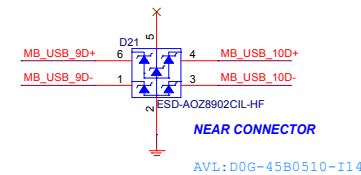
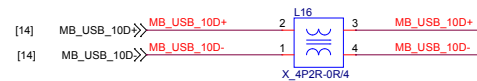
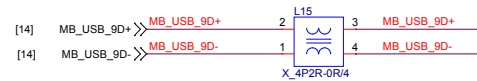
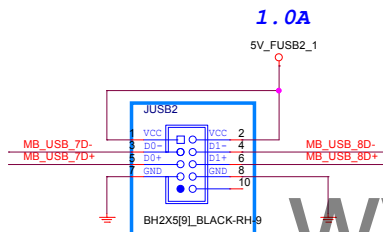
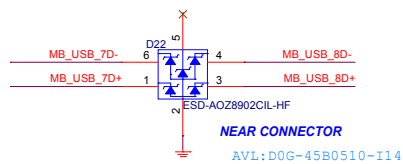
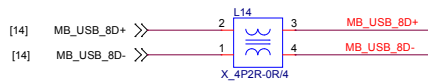
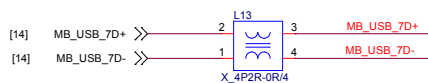
MICRO-STAR INT'L CO.,LTD
MS-7B58
Size Custom Document Description **USB TYPE C** Rev 10
Date: Monday, July 24, 2017 Sheet 28 of 72

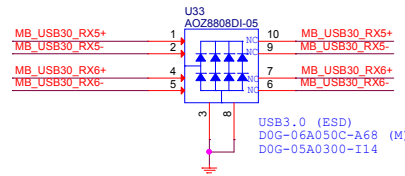
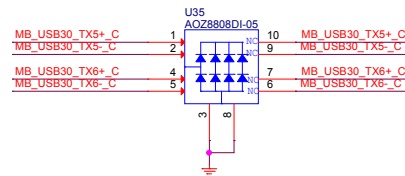
www.aitech1.ru



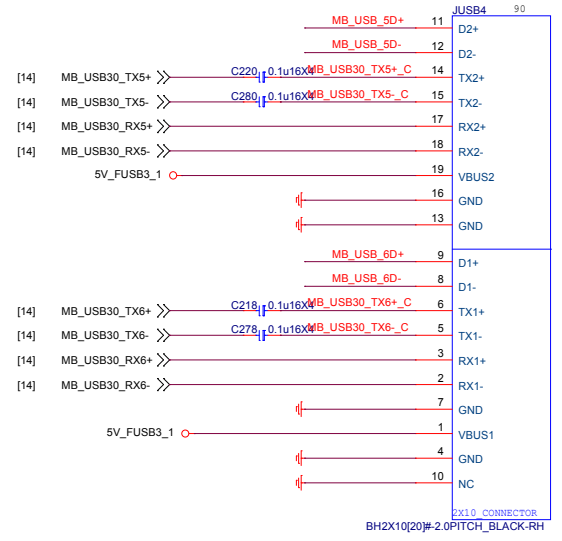
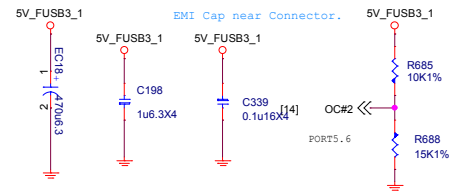
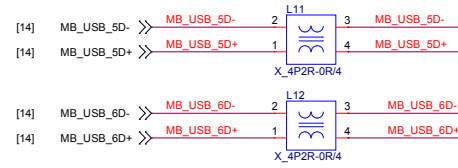
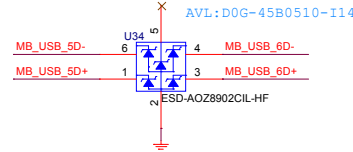
N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)



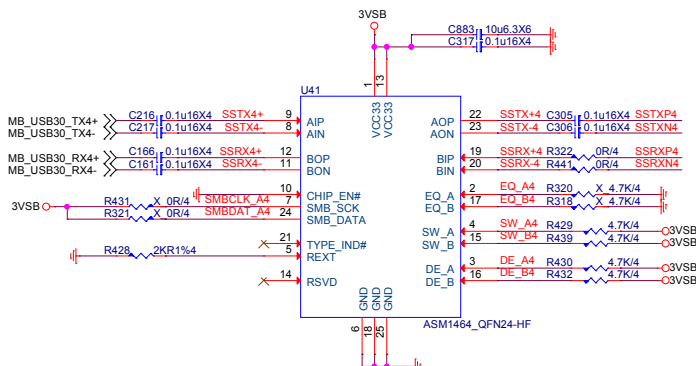
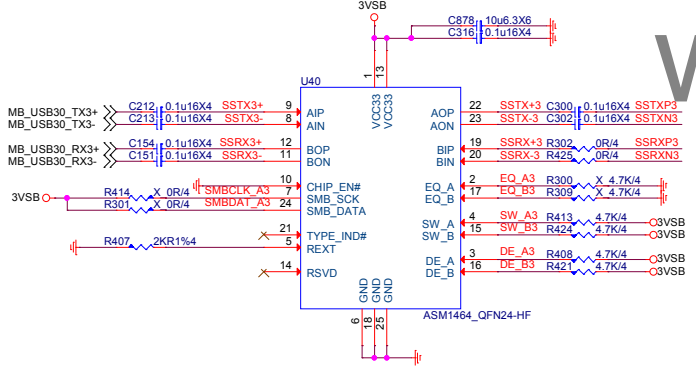


USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14

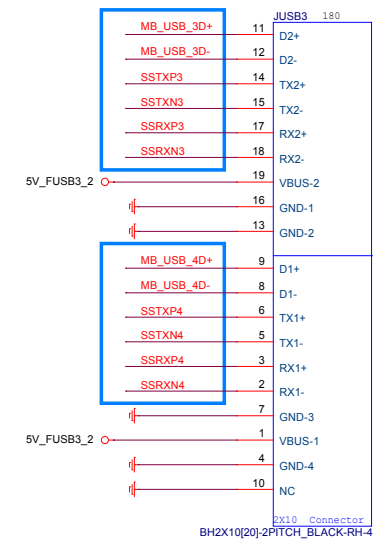
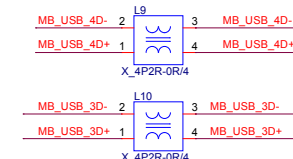
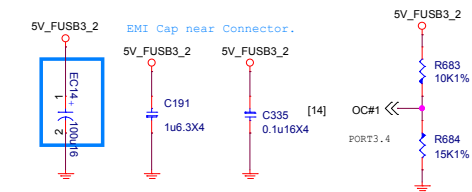
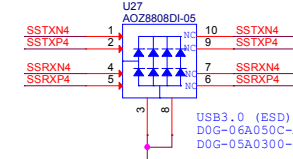
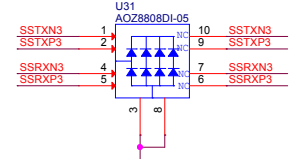


JUSB4 change to N32-2101581-H06.

www.aitech1.ru

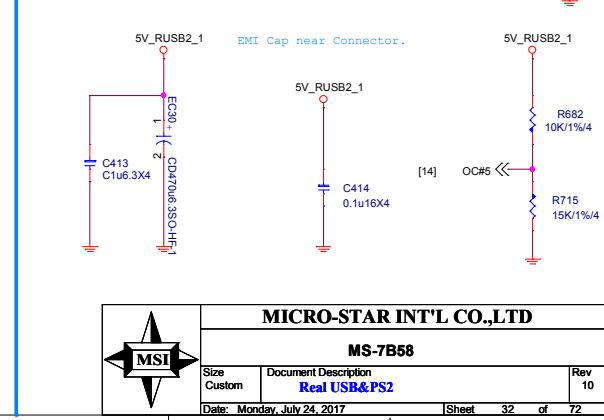
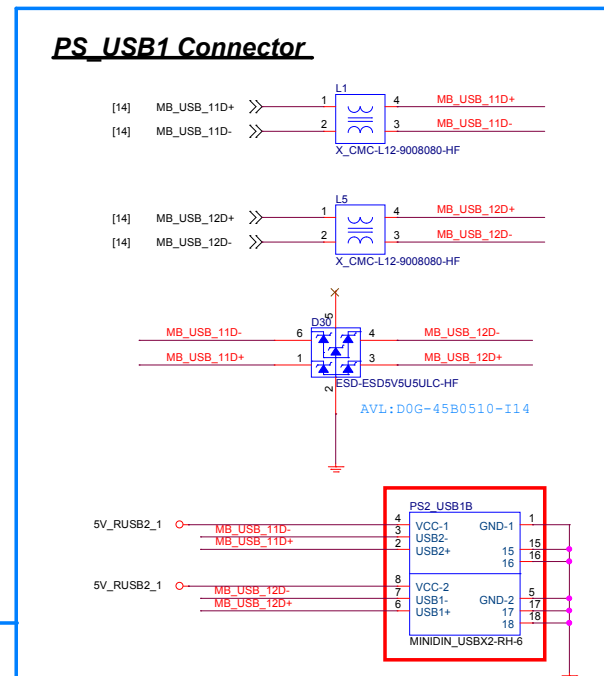
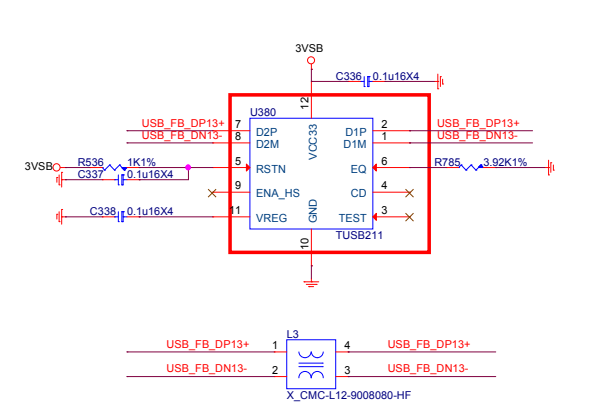
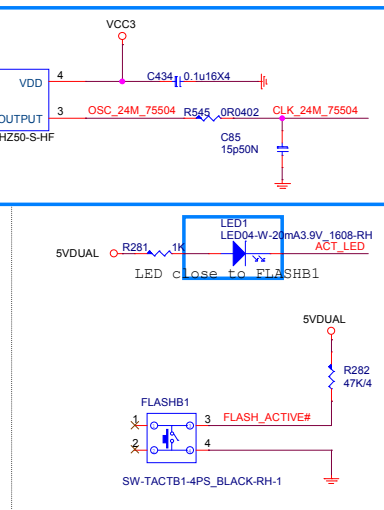
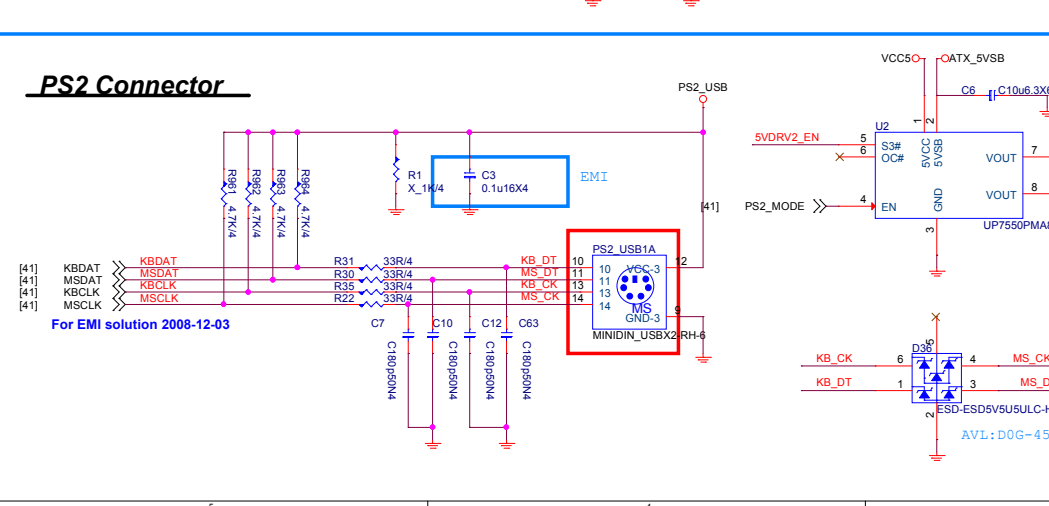
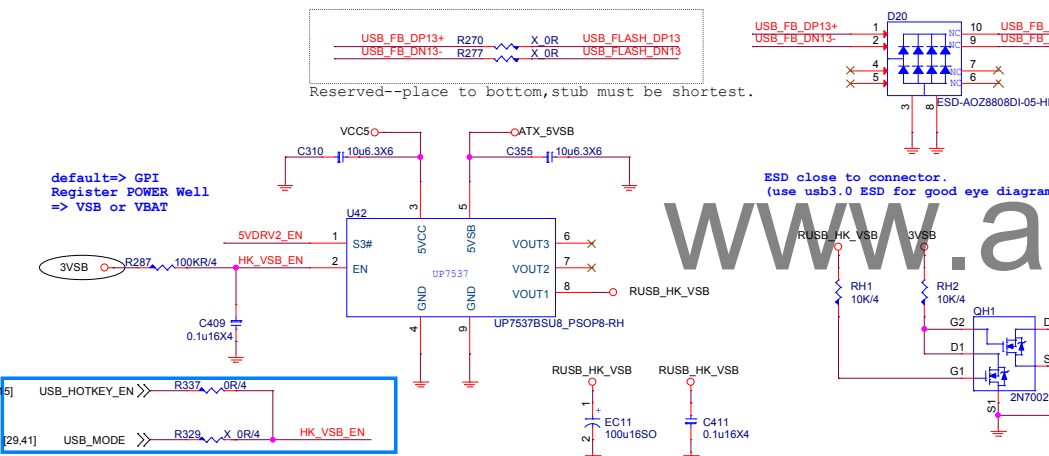
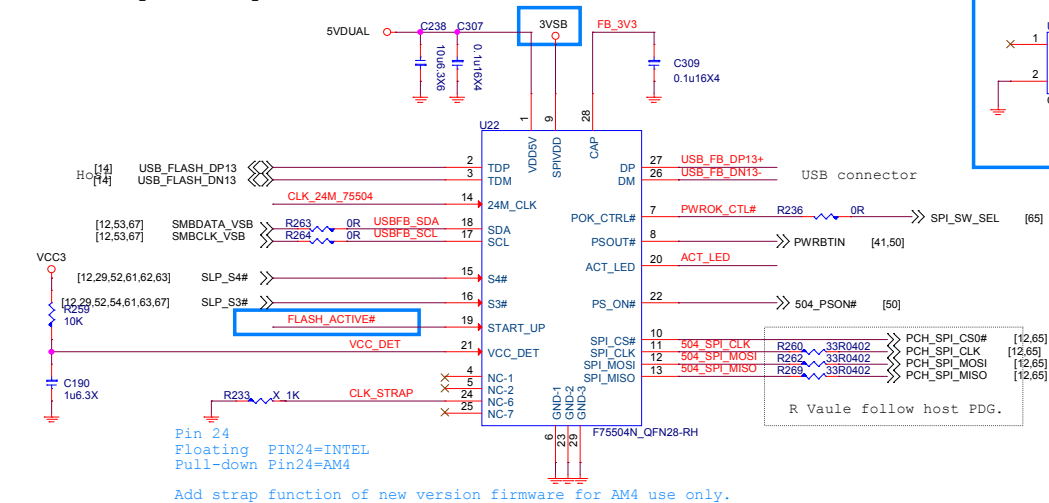


MB_USB_4D+ MB_USB_4D- MB_USB_4D+ MB_USB_4D-

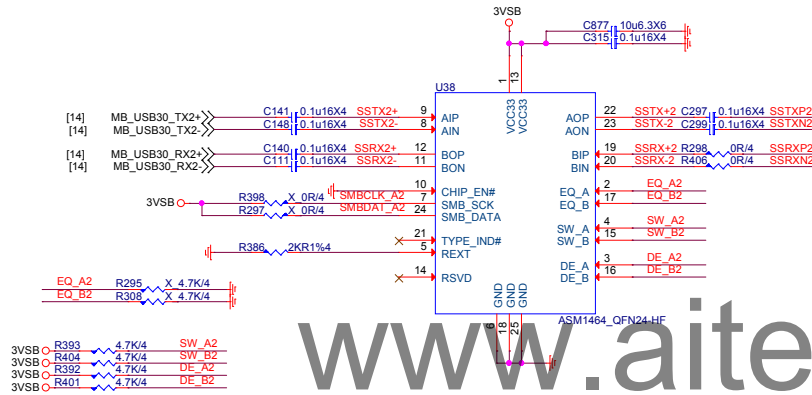
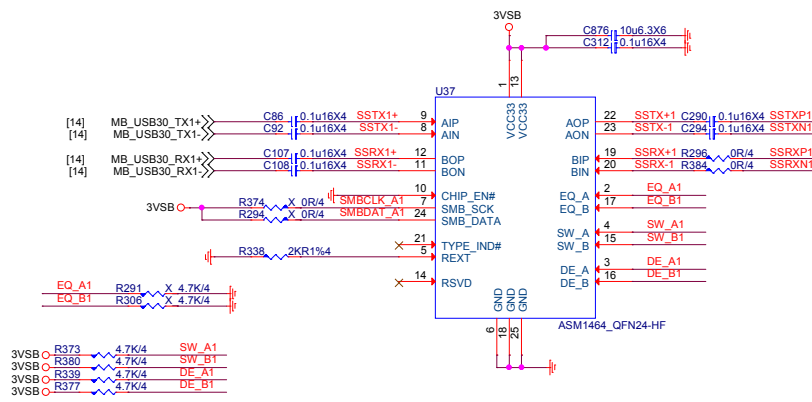


JUSB3 change to N32-2101091-H06.

F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

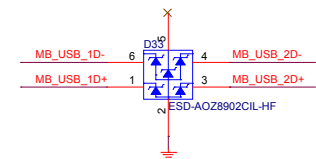
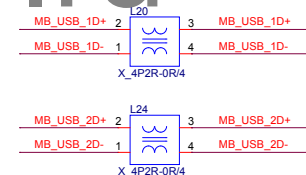
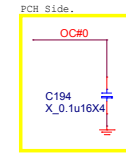
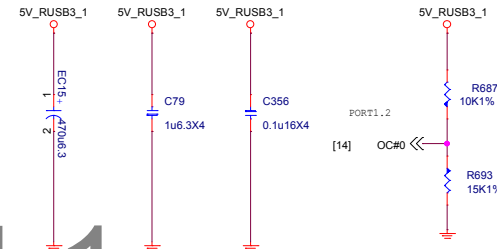
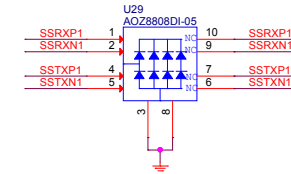
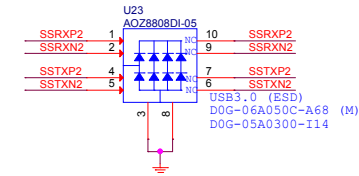


LAN USB3.0

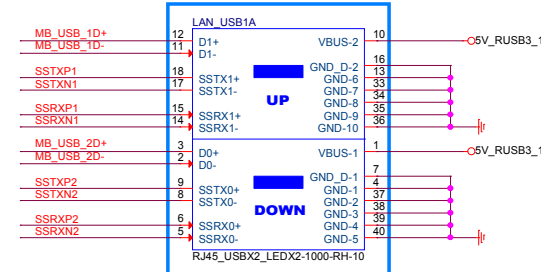


[14] MB_USB_1D+ MB_USB_1D-
[14] MB_USB_1D- MB_USB_1D+

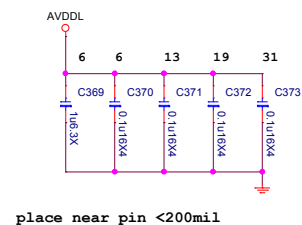
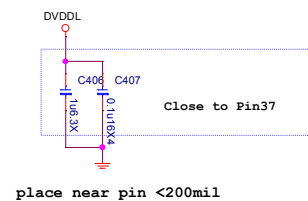
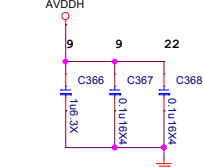
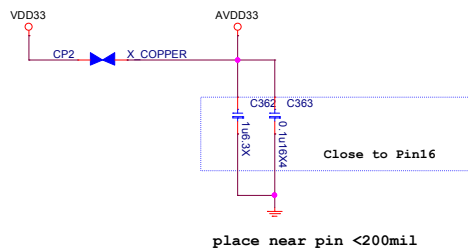
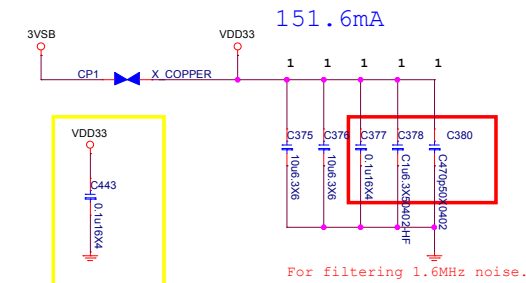
[14] MB_USB_2D+ MB_USB_2D-
[14] MB_USB_2D- MB_USB_2D+



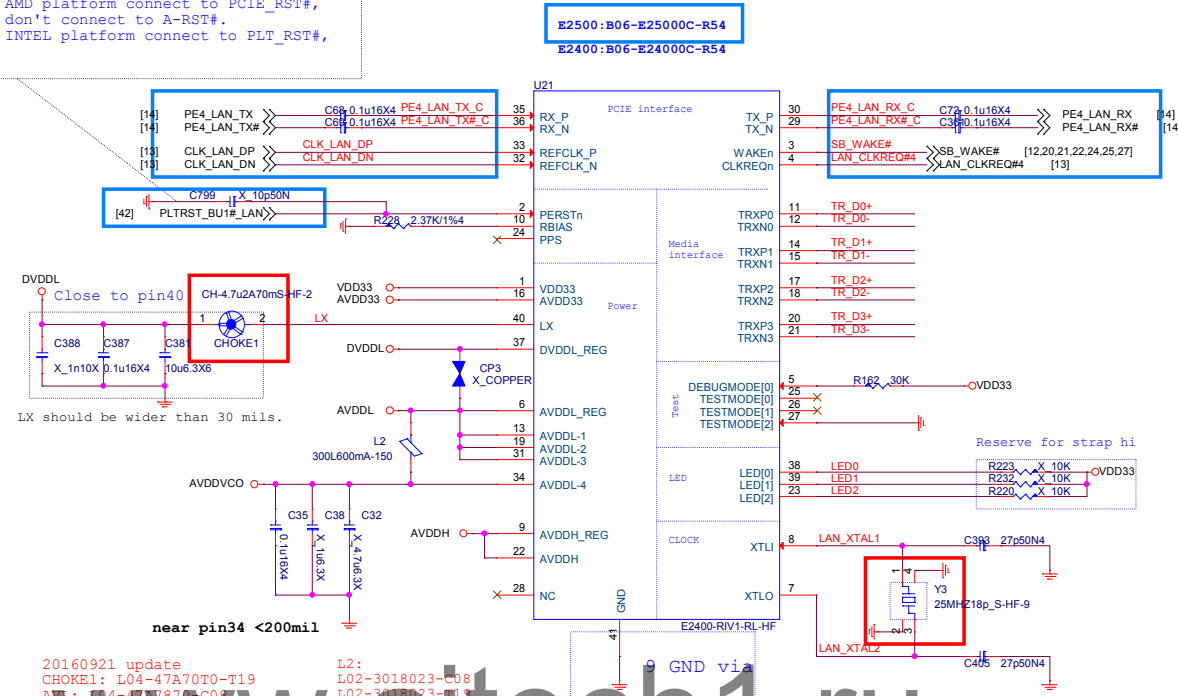
AVL:D0G-45B0510-I14



E2400 GIGA LAN



```
PIN2:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#.
```



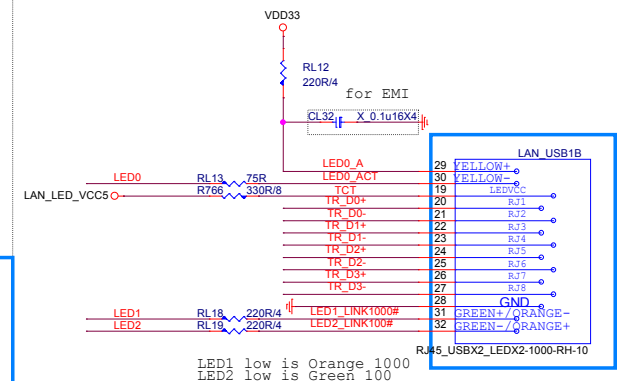
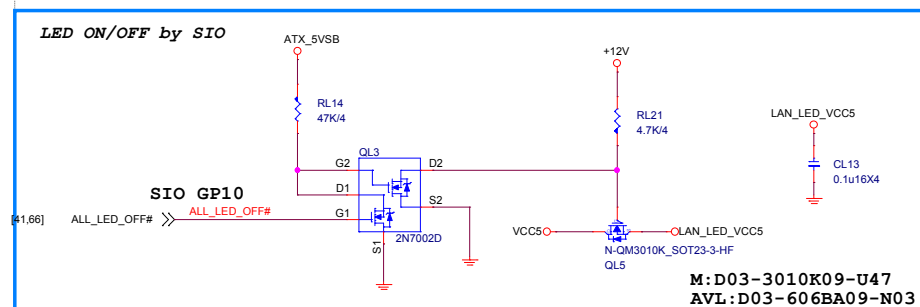
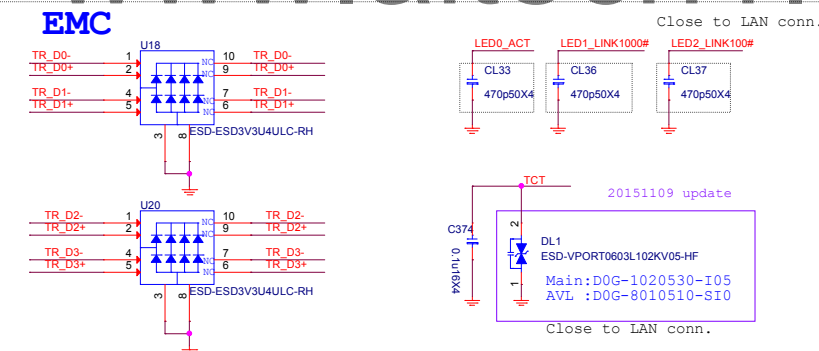
note:

```
LED0:
1=High core voltage
0=Low core voltage
```

```
LED1:
1=SWR mode
0=LDO mode
```

```
LED2:
1=25MHz  clock
0=48MHz  clock
```

```
VDD33 >= 30mils;  
AVDD33 >= 30mils;  
AVDDH >= 20mils;  
AVDDL >= 20mils.  
DVDDL >= 20mils.  
Pin LX to L1 >= 30mils.
```



MICRO-STAR INT'L CO.,LTD

MS-7B58

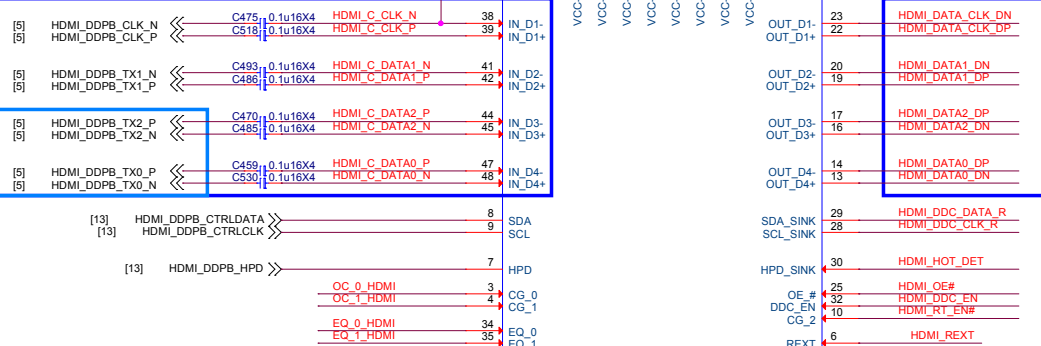
Size	Document Description	Rev
Custom	Killer Lan-E2400	10

Date: Monday, July 24, 2017	Sheet 34 of 72
-----------------------------	----------------

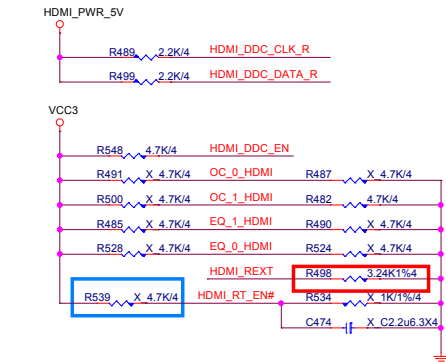
HDMI level shifter

Please CHECK R553 placement cannot let CLK- have stub

MAX Trace Length 5.5" reference to ground.



Note:DDSP_B_TX0 and TMDSB_DATA2 the same
Note:DDSP_B_TX2 and TMDSB_DATA0 the same
Note:IN_D and OUT_D the same



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

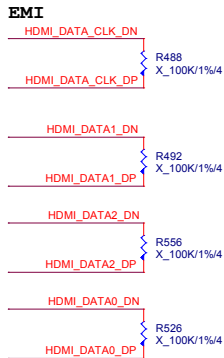
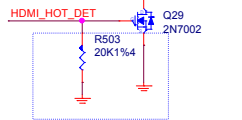
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

Level Shift to HDMI connector total trace length > 0.9" ; < 1" via count ≤ 2 ,reference to ground.

www.aitech1.ru

注意High/Low Detect



EMI cap.

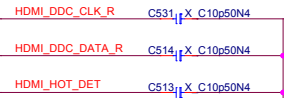
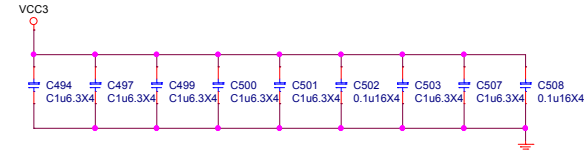
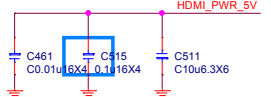
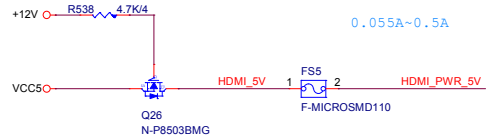
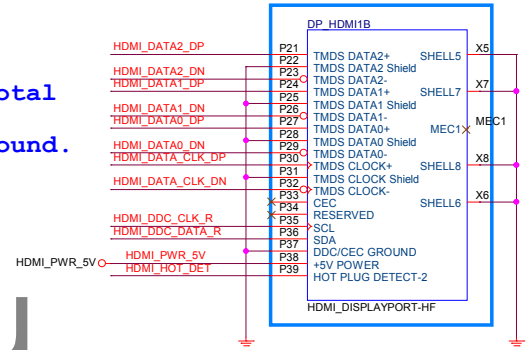
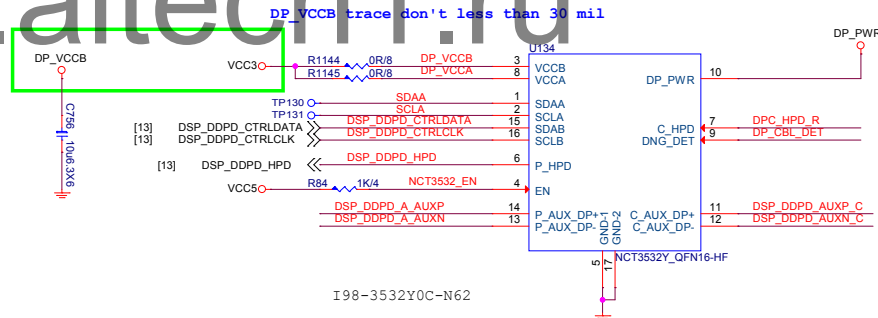
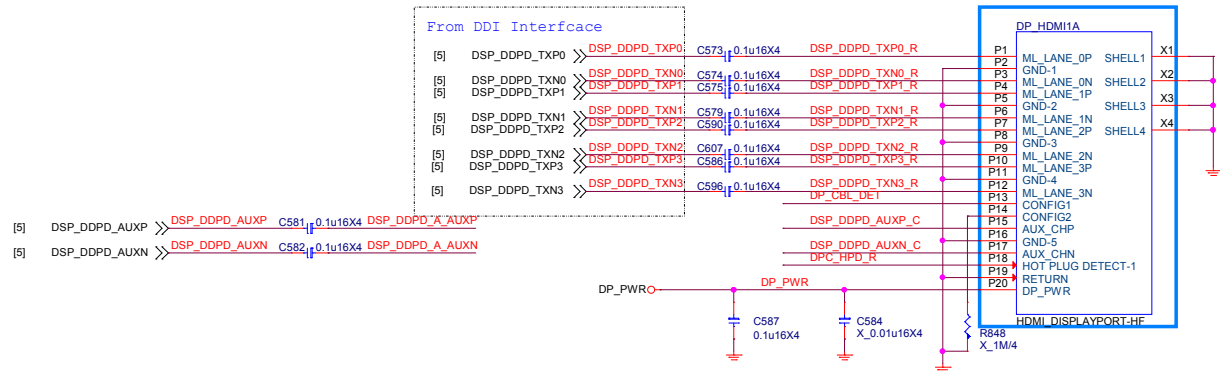
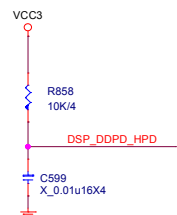
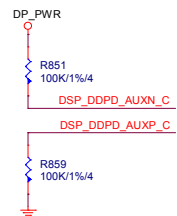
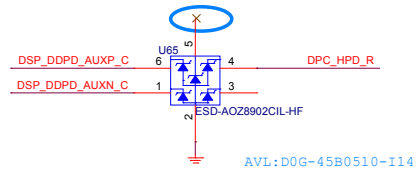
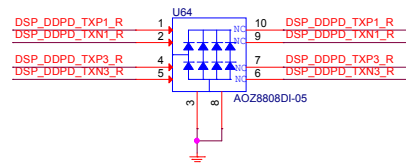
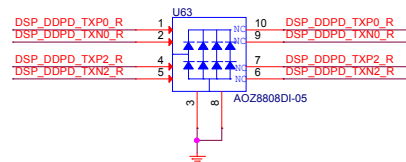


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

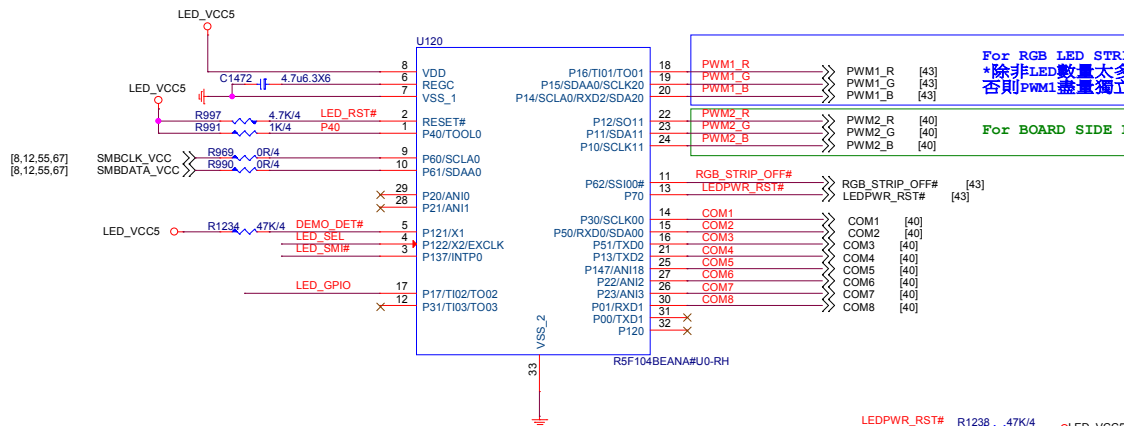


MICRO-STAR INT'L CO.,LTD			
MS-7B58			
Size	Document Description	Rev	
Custom	DP_HDMI Connector	10	
Date: Monday, July 24, 2017		Sheet	35 of 72



www.aitech1.ru

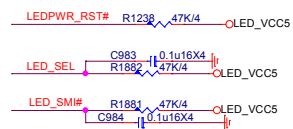
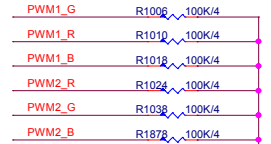
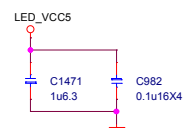
LED MCU



For RGB LED STRIPLINE --> PWM1
*除非LED數量太多
否則PWM1盡量獨立給RGB LED STRIPLINE做使用

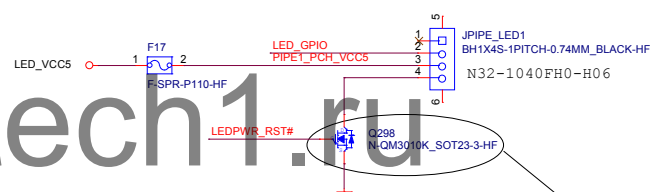
For BOARD SIDE LED*8 --> PWM2

Control	Net Name	PWM USE
PCH	LED_GPIO	PWM3
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
LED STRIPLINE	RGB_STRIP_OFF#	PWM1
Board Side LED	COM X-8	PWM2
PCIE Side LED	COM 1-X	PWM1



1 PCH HEATSINK LED

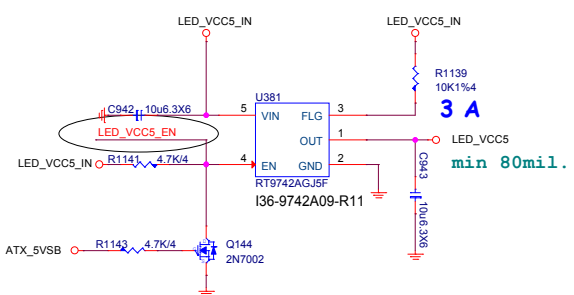
8PCS LED*0.16W=1.28W PIPE1_PCH_VCCS need 20mil



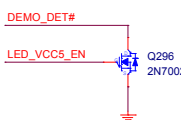
If JPIPE module doesn't has LED driver IC then can remove these MOS.

Delete JPIPE2/3
(Audio/IO cover LED CONN.)
BY PM spec

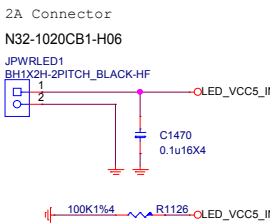
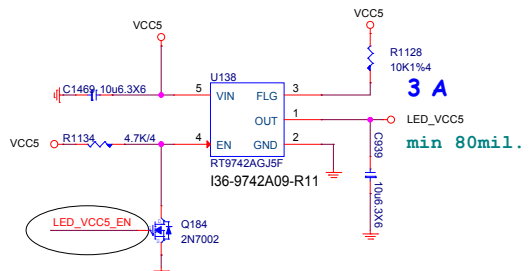
EXTERNAL POWER INPUT



LED Demo Button

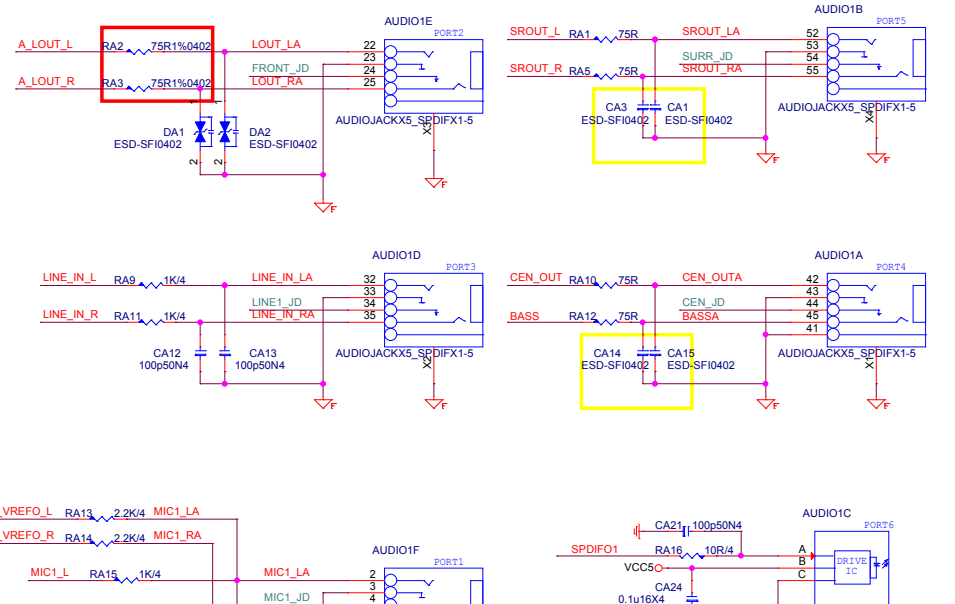
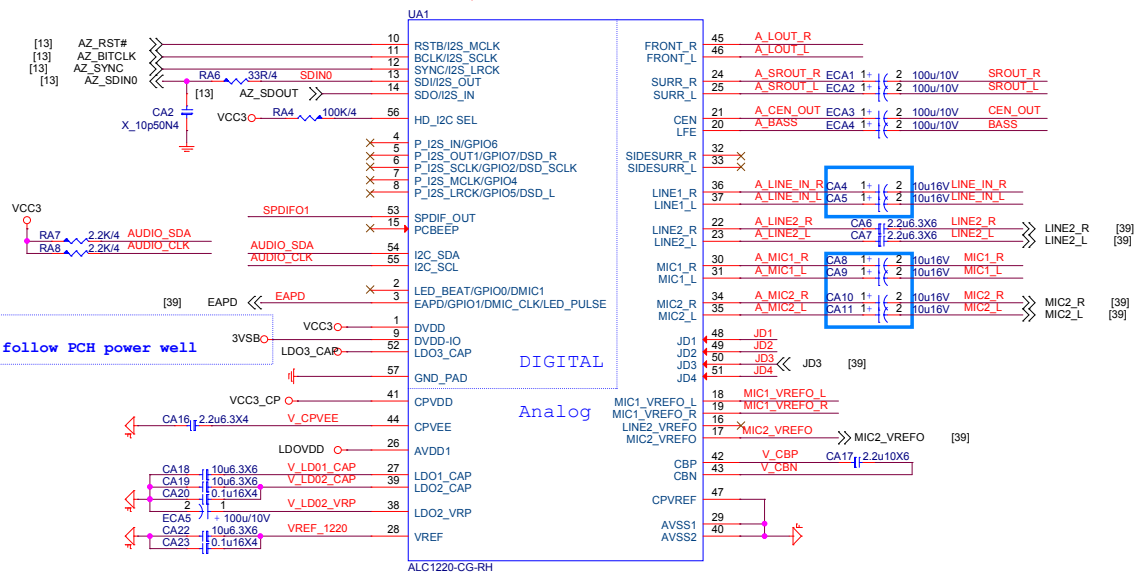


External Power

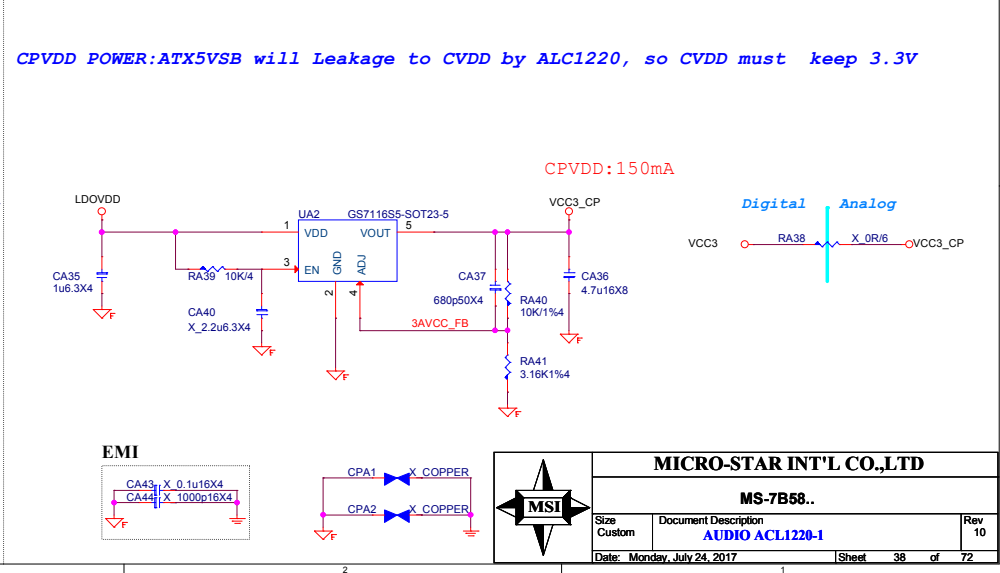
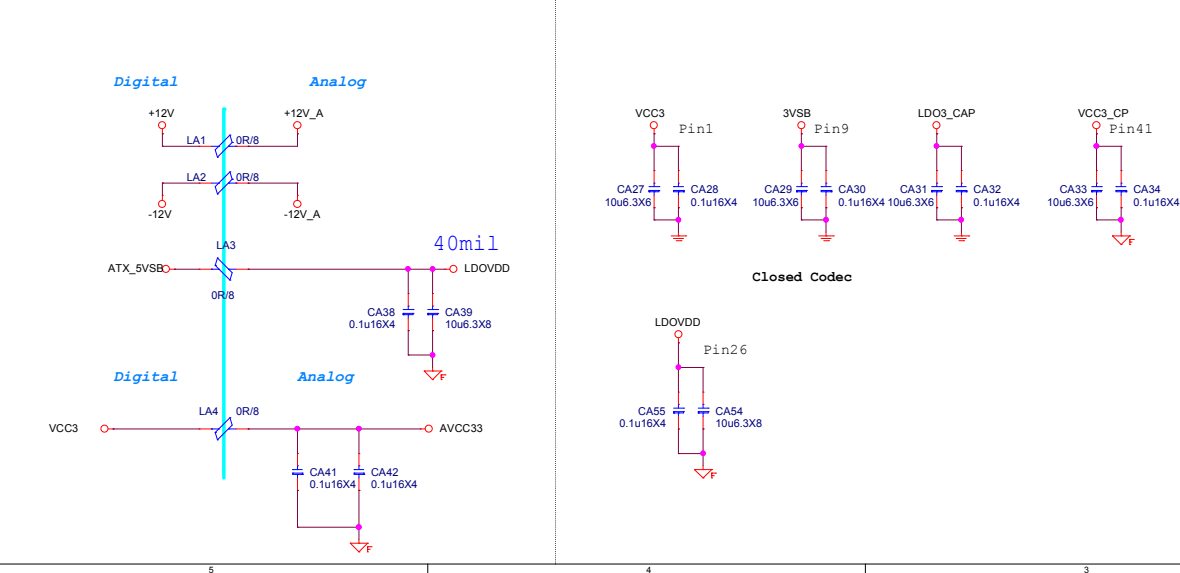
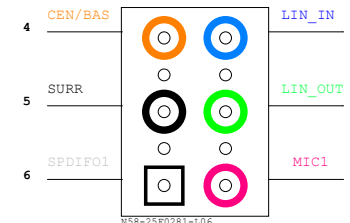


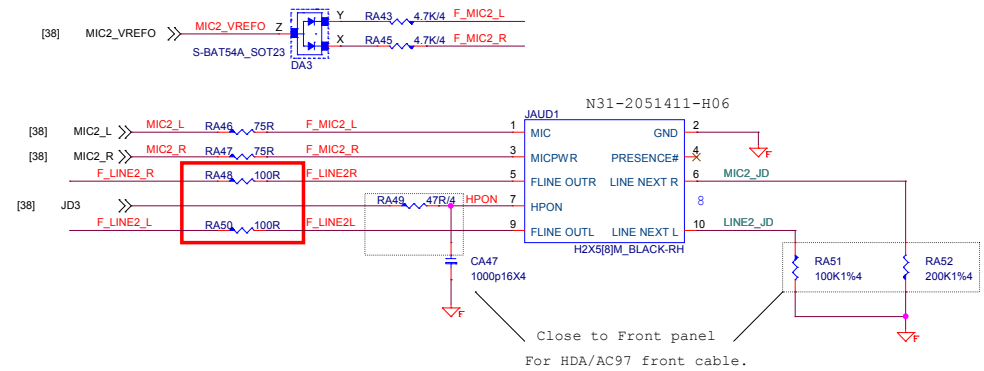
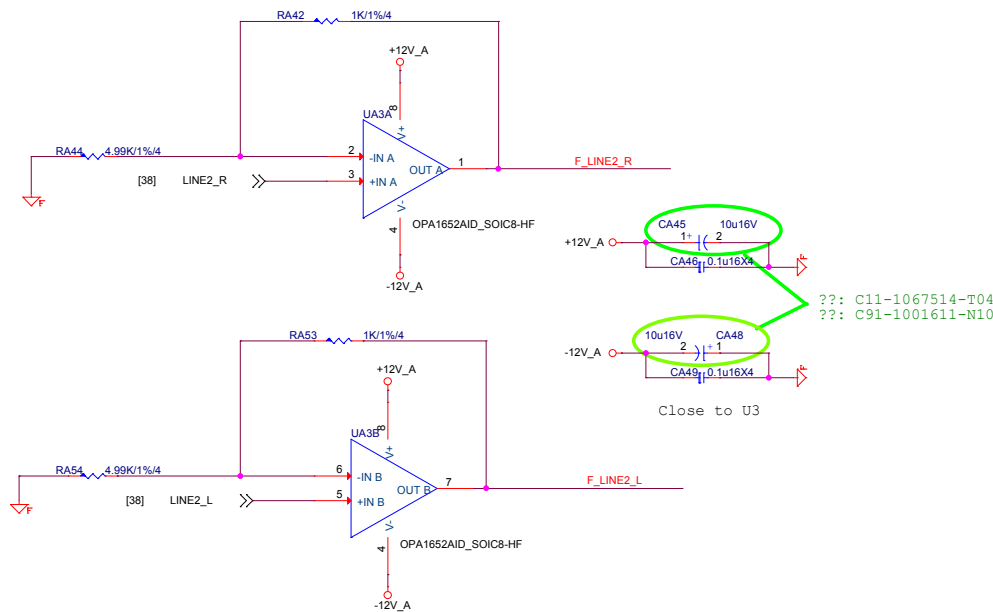
ALC1220

P/N:B05-012201C-R09



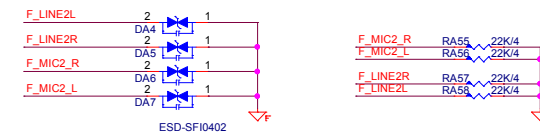
www.aitech1.com





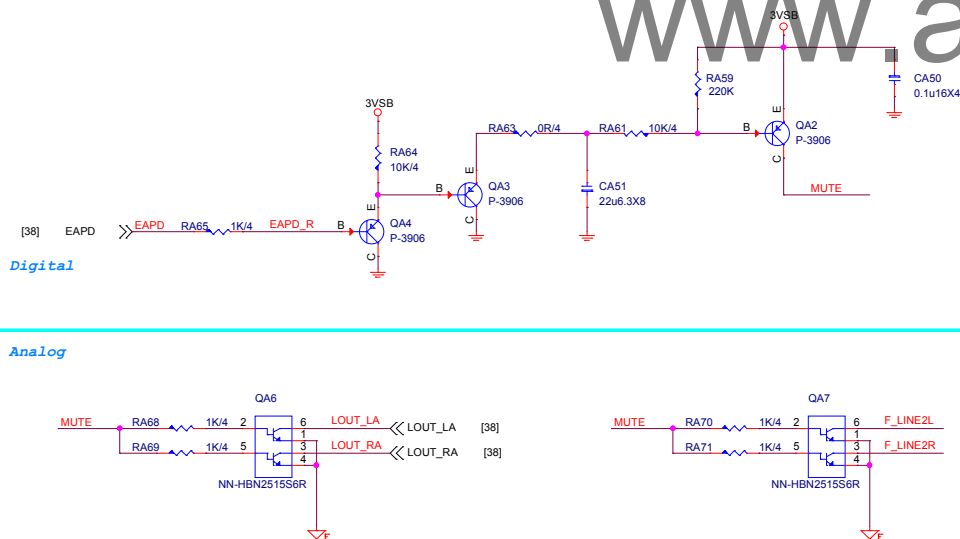
Close to Jack

ESD protect
D0G-2950500-S10
D0G-3010510-I05

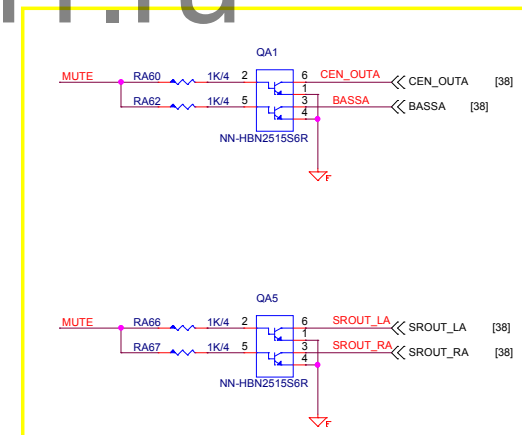


Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

www.aitech1.ru



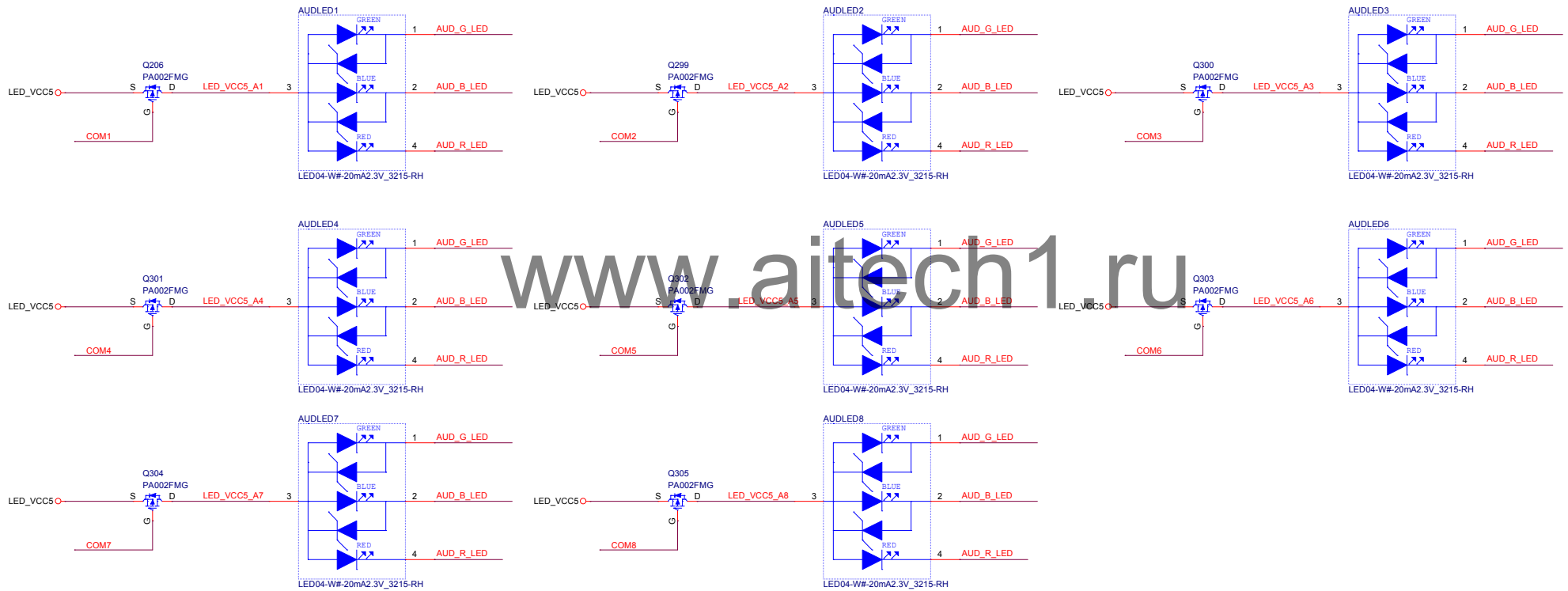
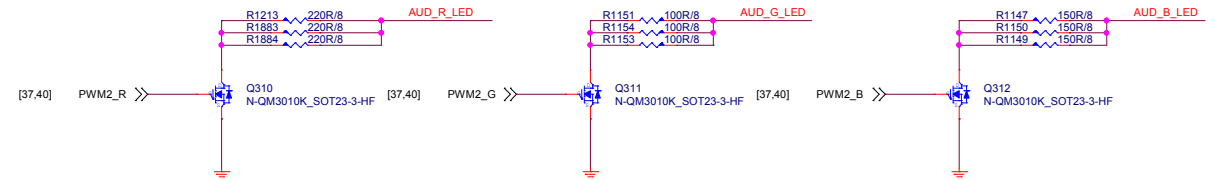
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



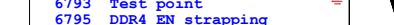
Audio moat is transparent and width 40mil

[37] COM1
[37] COM2
[37] COM3
[37] COM4
[37] COM5
[37] COM6
[37] COM7
[37] COM8

[37,40] PWM2_R
[37,40] PWM2_G
[37,40] PWM2_B

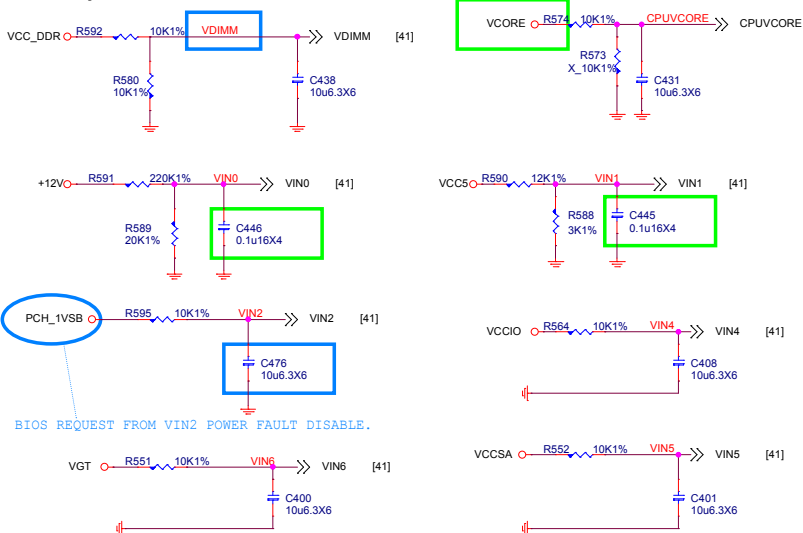


IF INTEL DSW ENABLE
Other unused pin can be other function
(EX:GPIO)



HW Monitor - Voltage

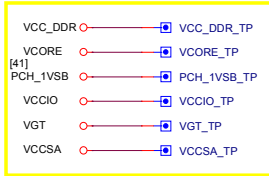
SIO HM Voltage voer 2V will not detect



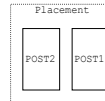
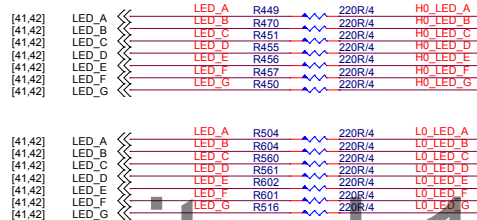
BIOS REQUEST FROM VIN2 POWER FAULT DISABLE.

SERIAL PORT 1

Z370 Modify; PM Spec change

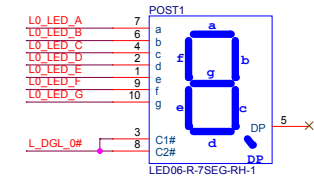
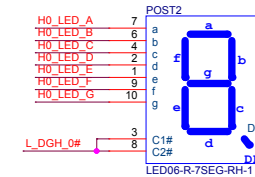


Debug LED

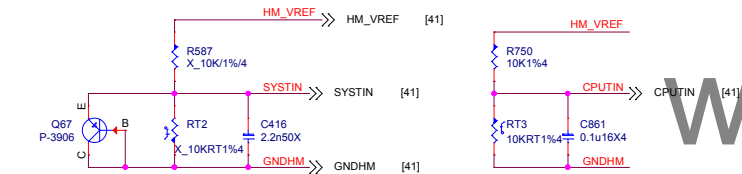


Placement一定要對 (DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

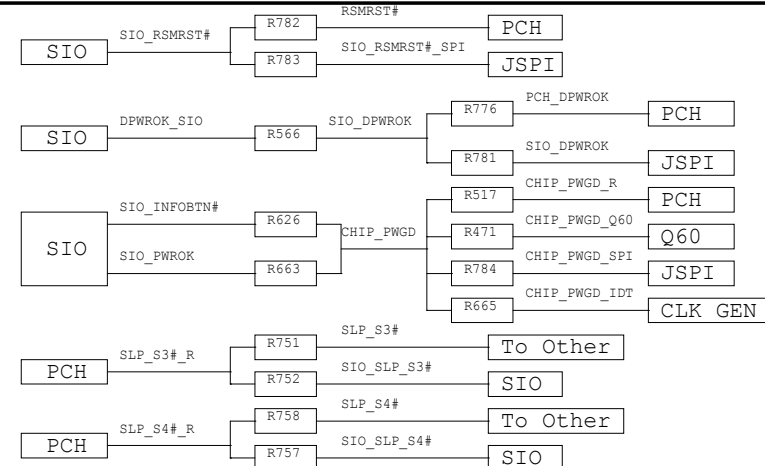
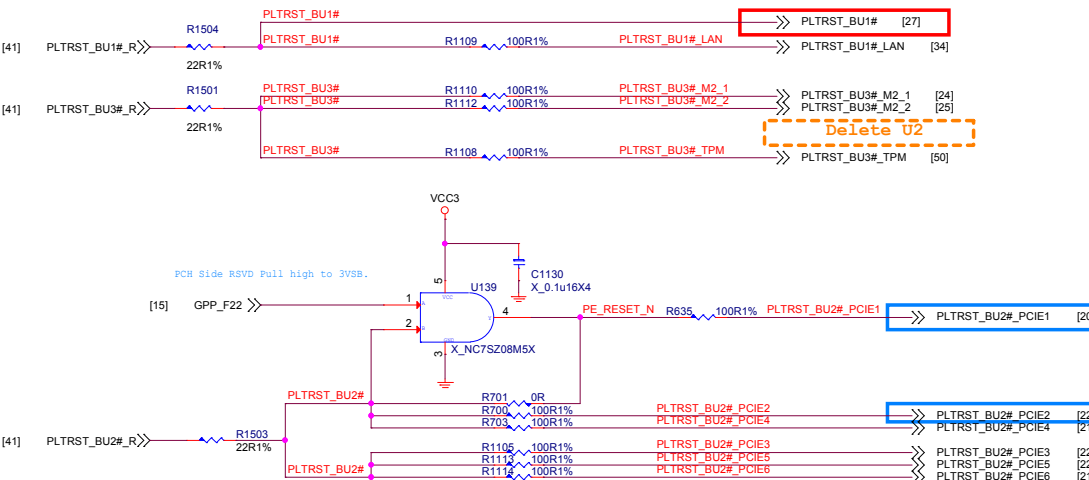
Debug LED OFF BIOS control



Thermal Monitor



www.aitech1.ru

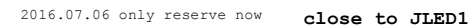


For Signals Monotonic

2016.07.06 Use TPS25944L

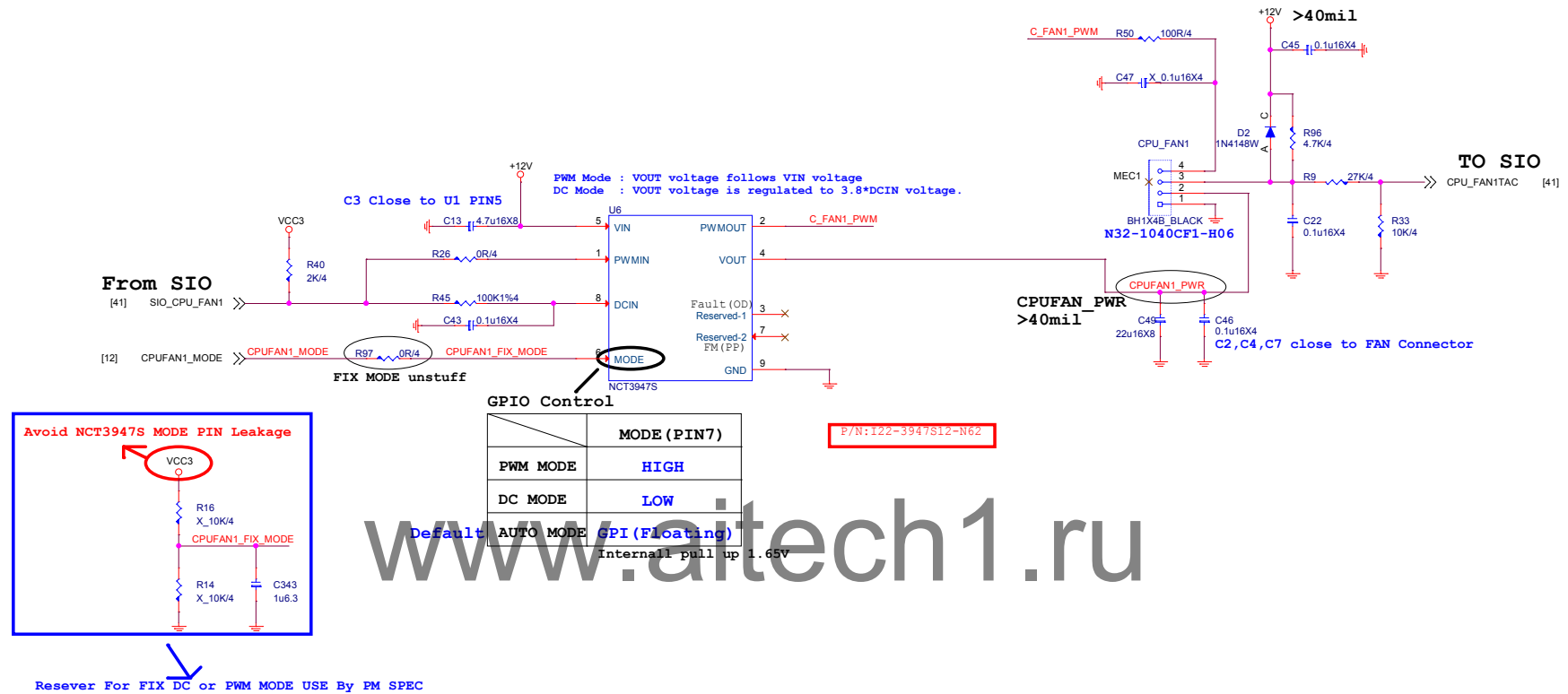


Change location to JRGB1 form JLED1
By PM request



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE



2.GPIO可以由BIOS切換 PWM/DC MODE

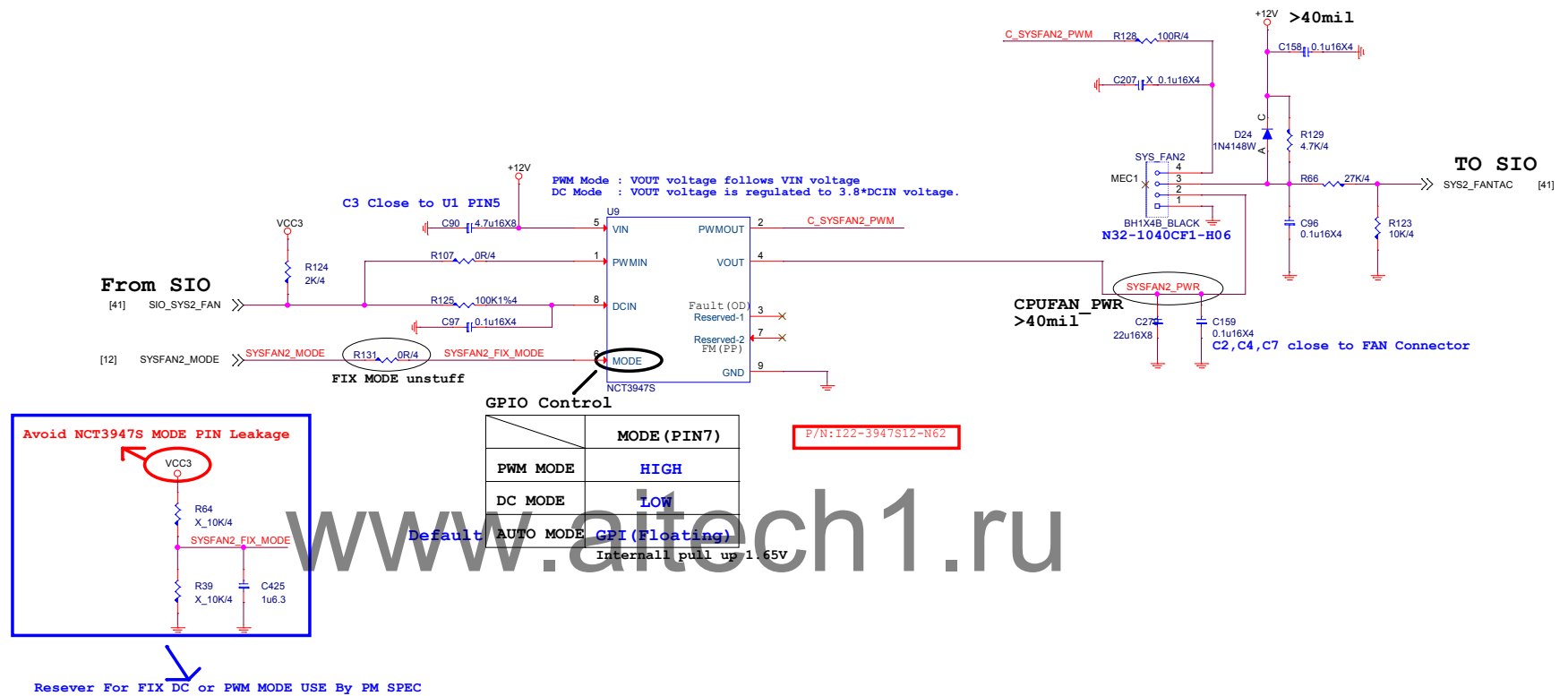


2. GPIO可以由BIOS切換 PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

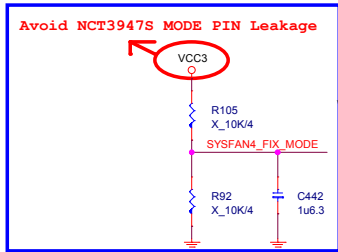
2.GPIO可以由BIOS切换 PWM/DC MODE



2.GPIO可以由BIOS切換 PWM/DC MODE

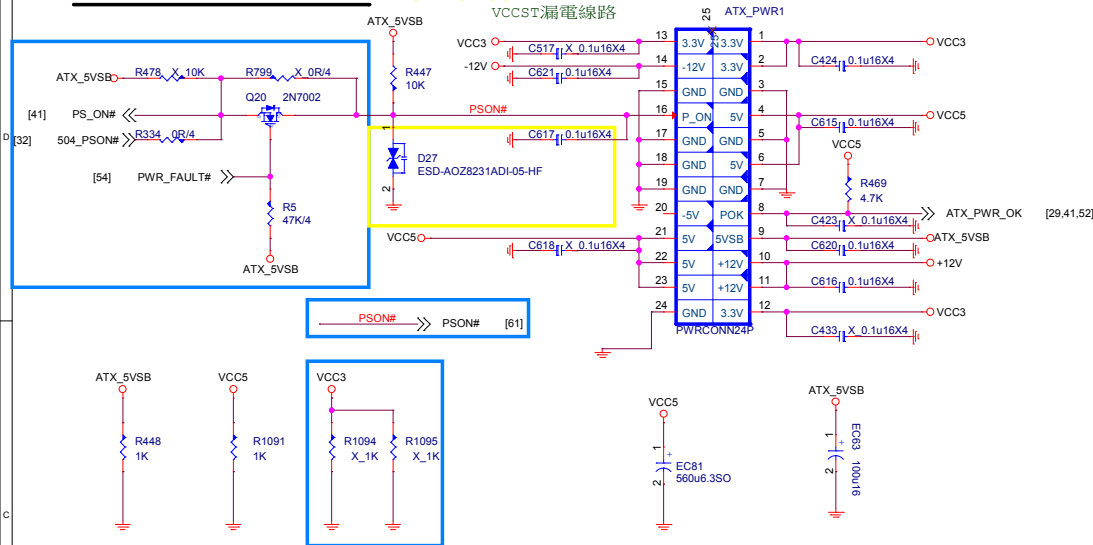


2.GPIO可以由BIOS切換 PWM/DC MODE

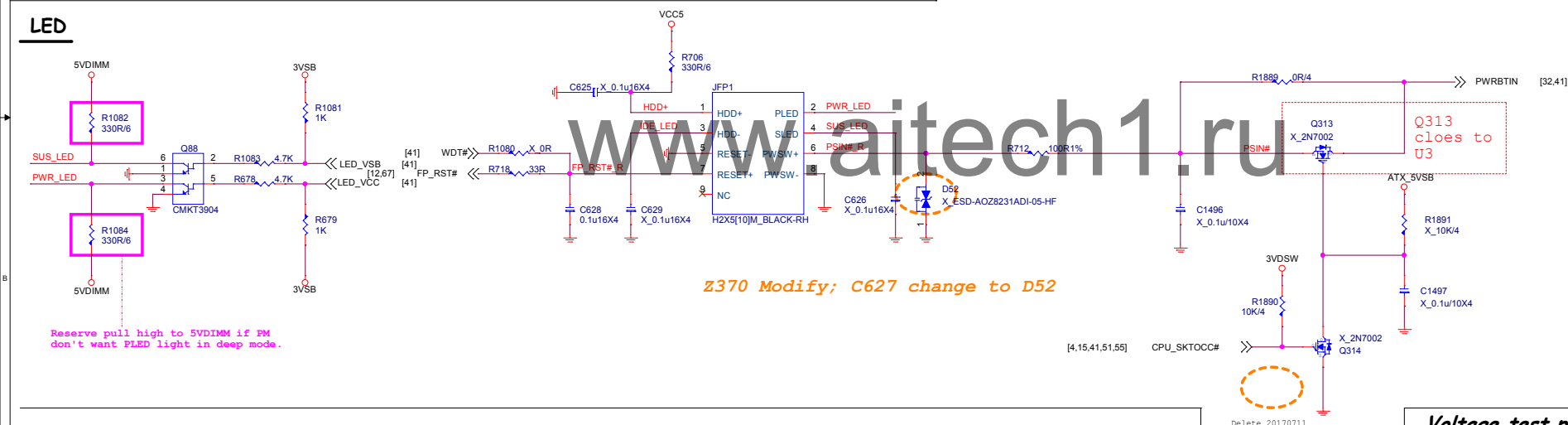


Resever For FIX DC or PWM MODE USE By PM SPEC

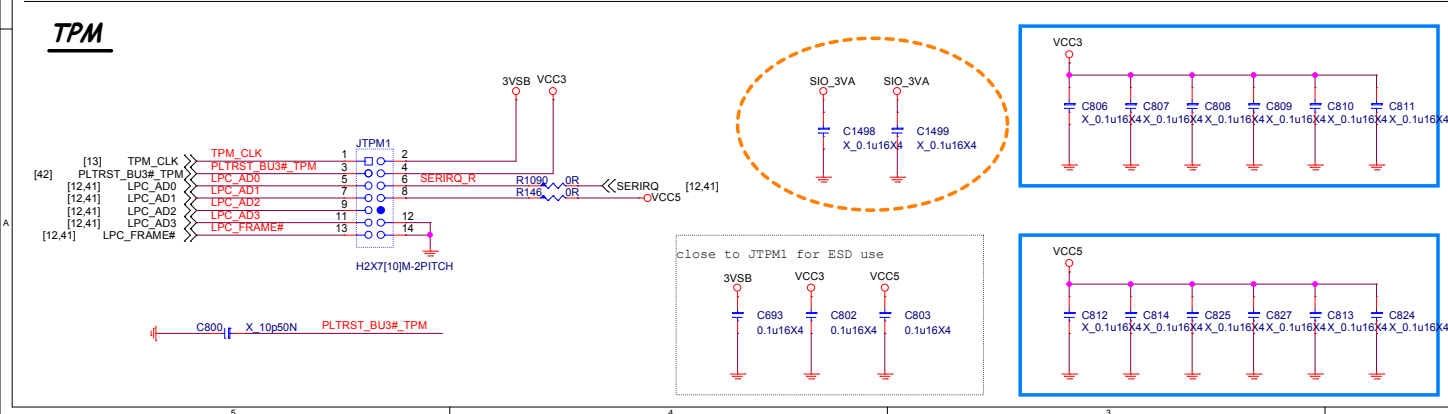
ATX POWER CONNECTOR 20170209



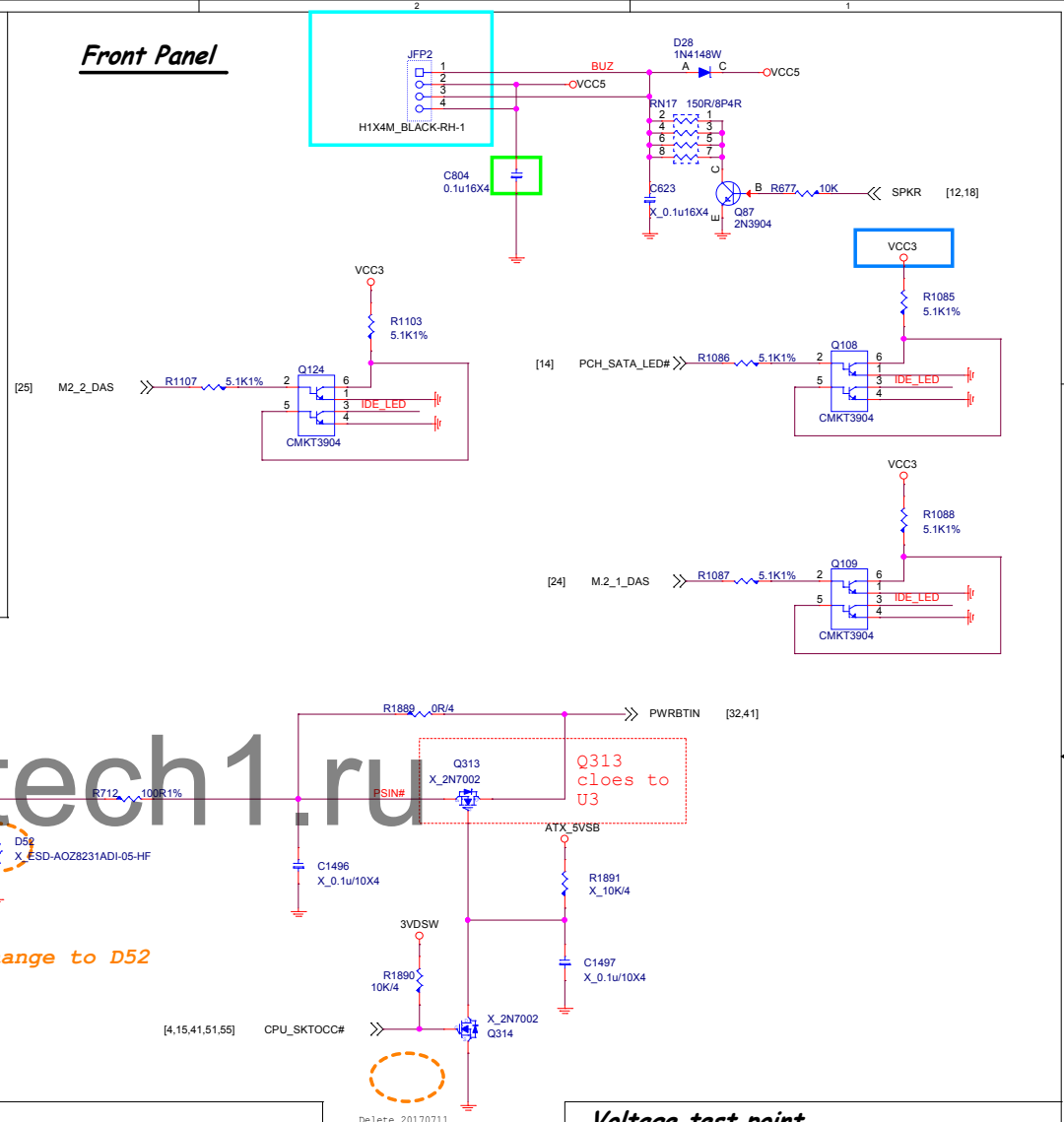
LED



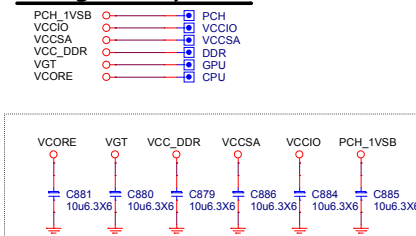
TPM



Front Panel



Voltage test point



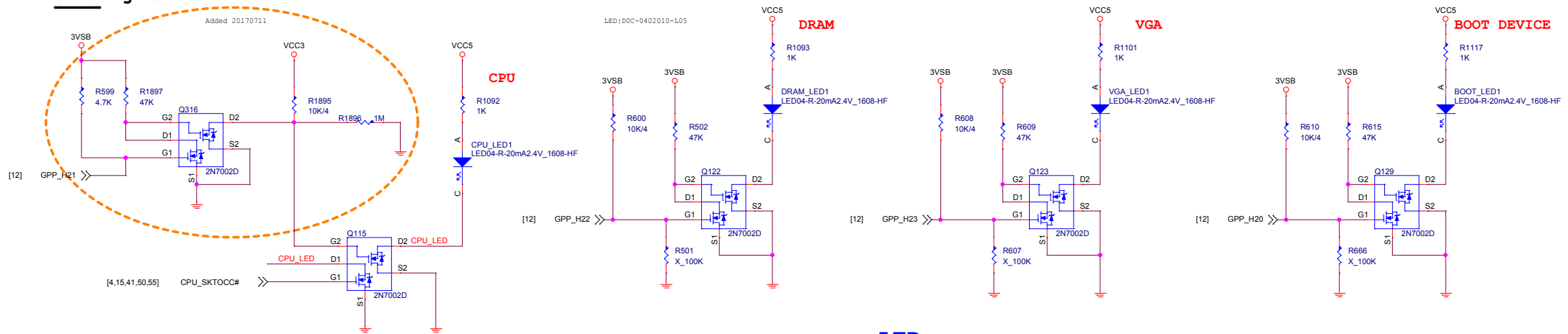
MICRO-STAR INT'L CO.,LTD

MS-7B58

Size Custom	Document Description ATX Power/F_Panel	Rev 10
Date: Monday, July 24, 2017		Sheet 50 of 72

EZ Debug LED

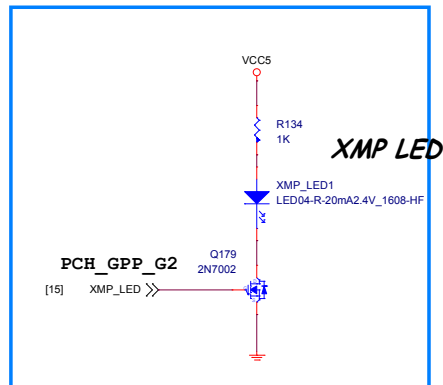
Added: 20170711



LED
紅 : D0C-040P100-H91

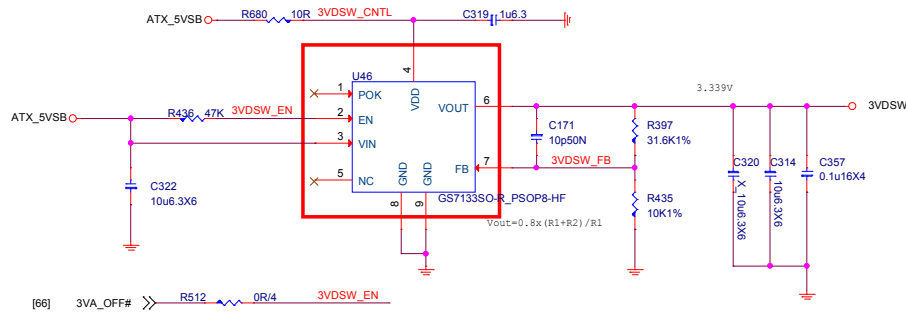
GPIO LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

www.aitech1.ru



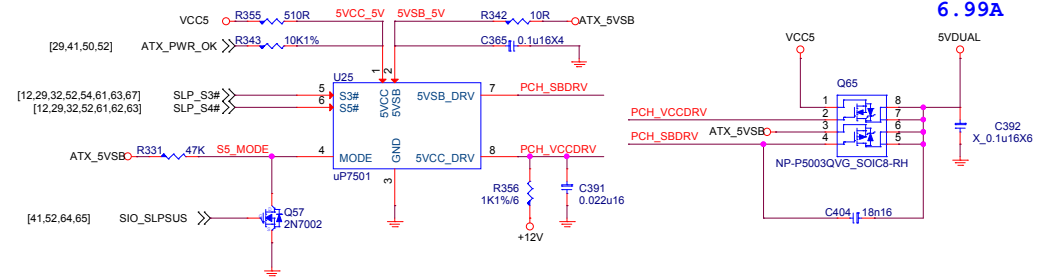
LED
紅 : D0C-040P100-H91

3VDSW



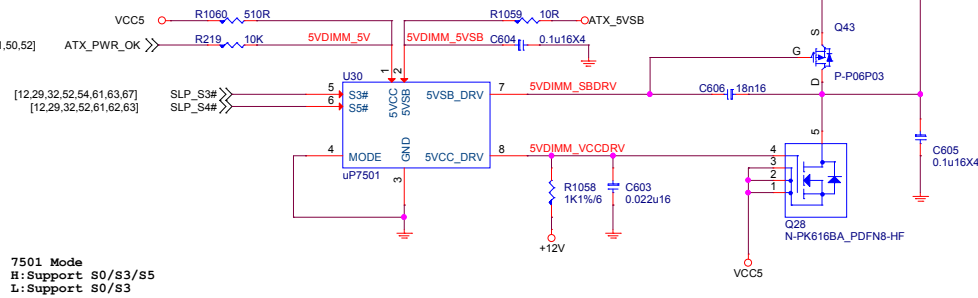
5VDUAL

5VDUAL is power source of 1P0SB



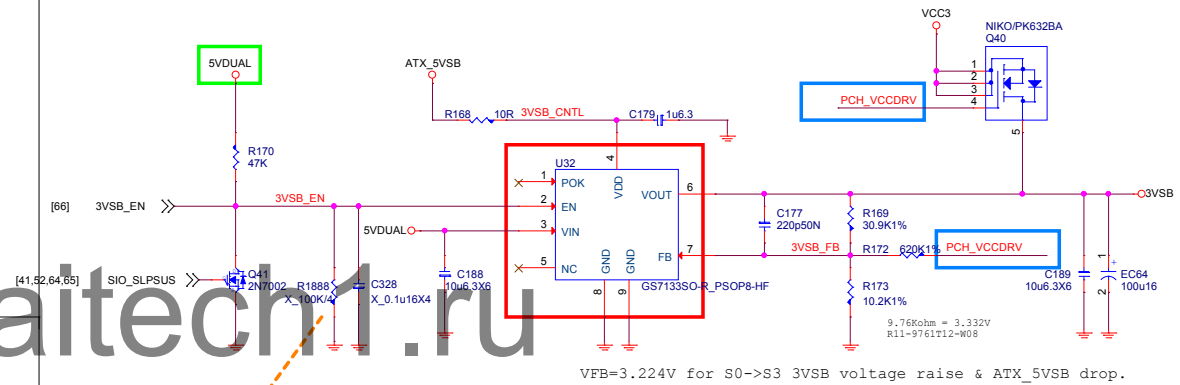
6.99A

5VDIMM FOR DDR



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

3VSB cost down



VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

Z370 Modify; Add Delay

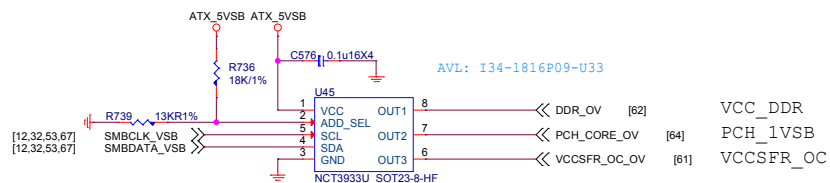


MICRO-STAR INT'L CO.,LTD

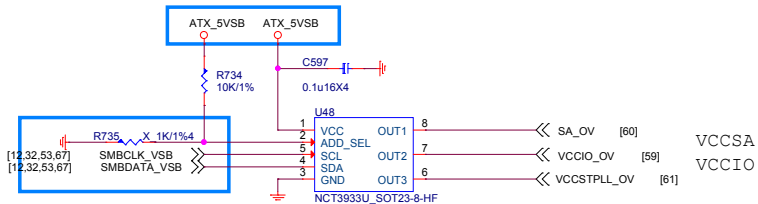
MS-7B58

Size Custom	Document Description ACPI UPI	Rev 10
Date: Monday, July 24, 2017	Sheet 52 of 72	

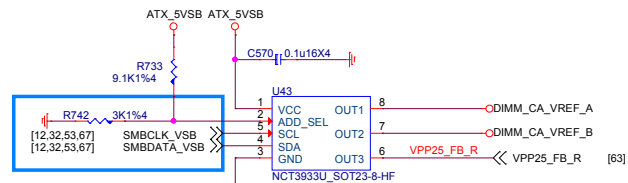
0x26: RH=18K, RL=13K



0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

CHB VREF

VP25

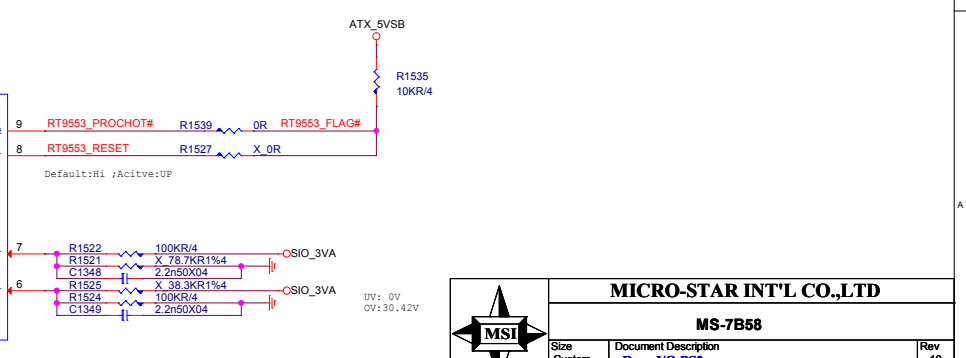
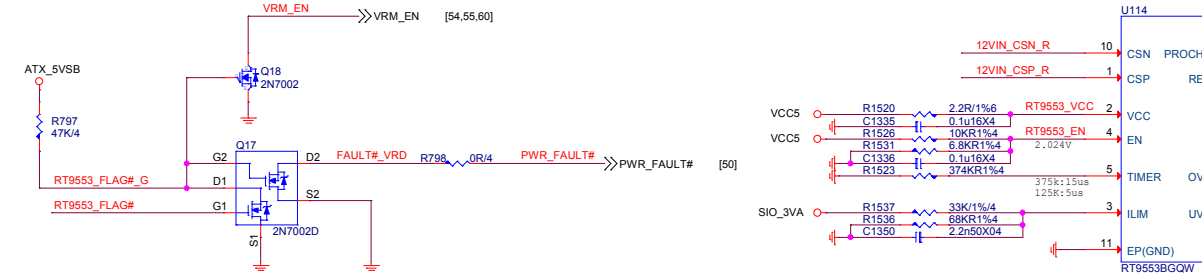
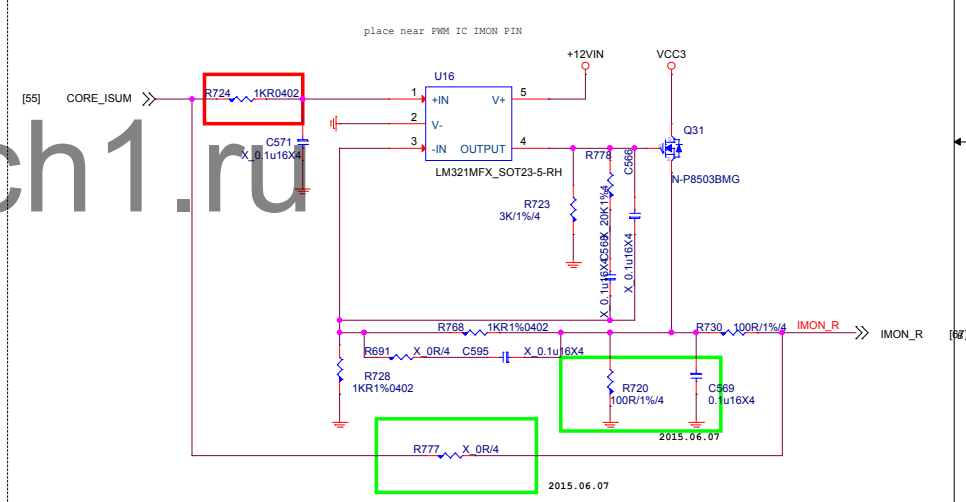
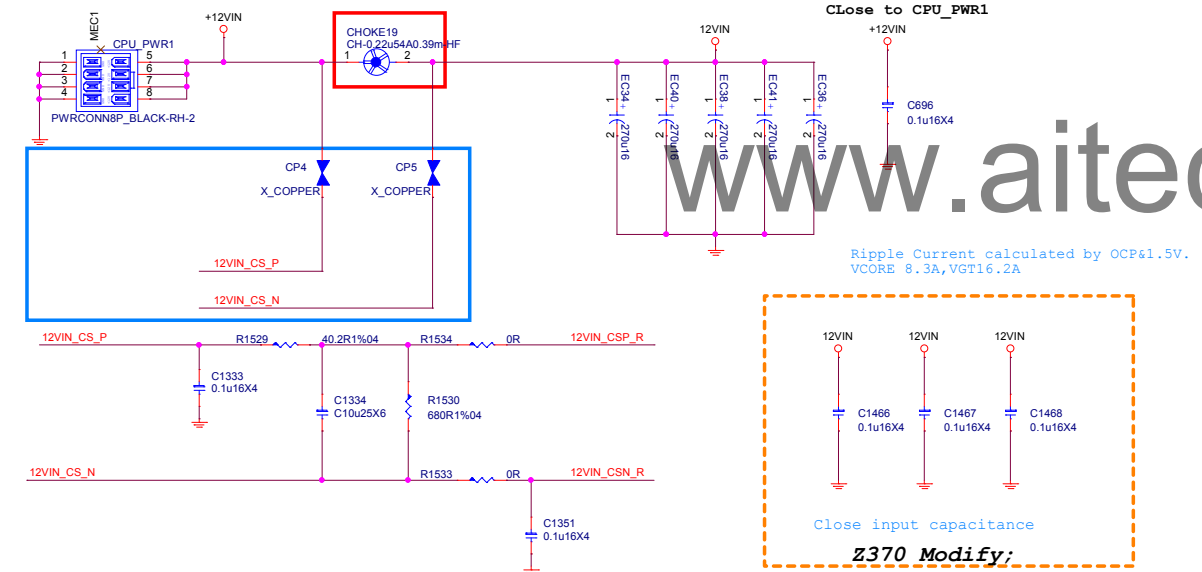
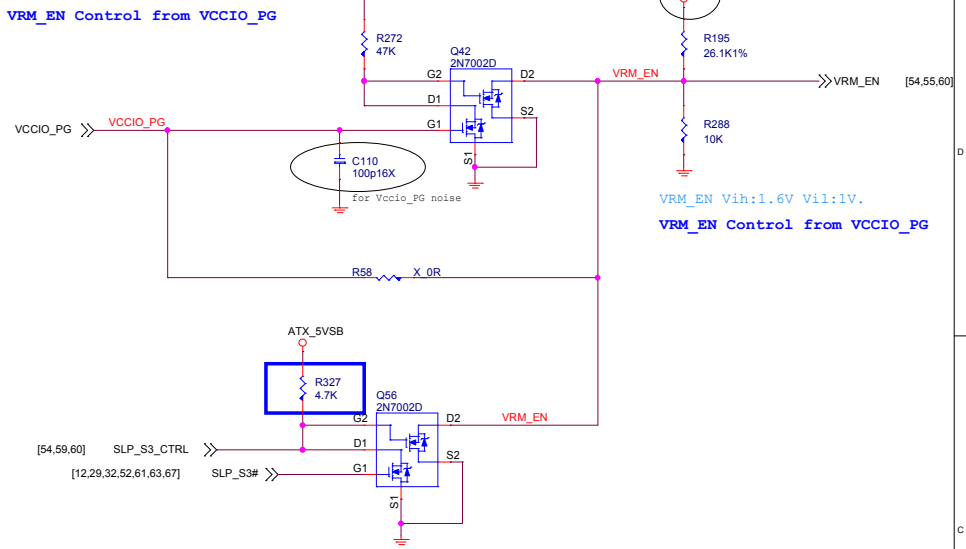
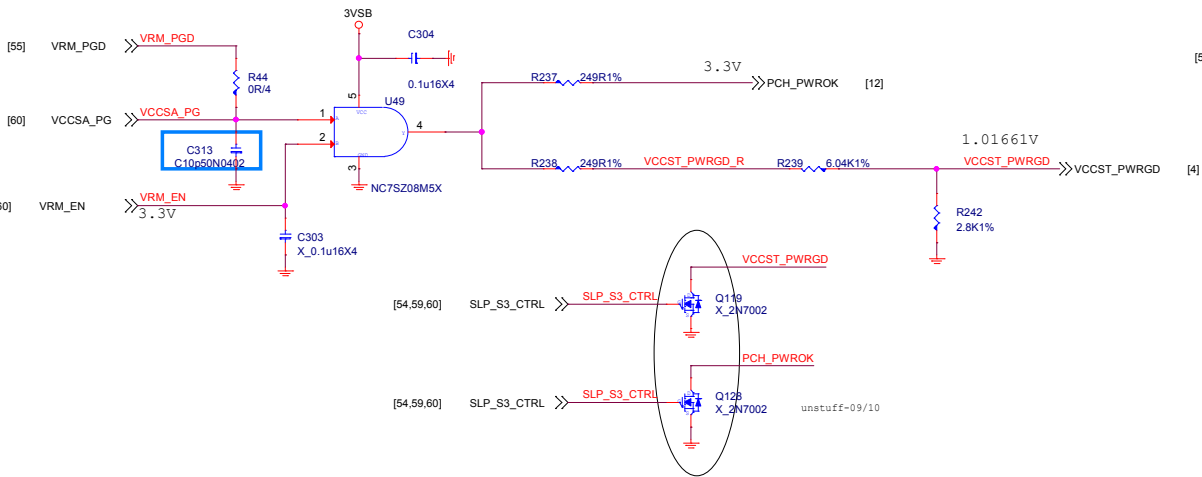
www.aitech1.ru



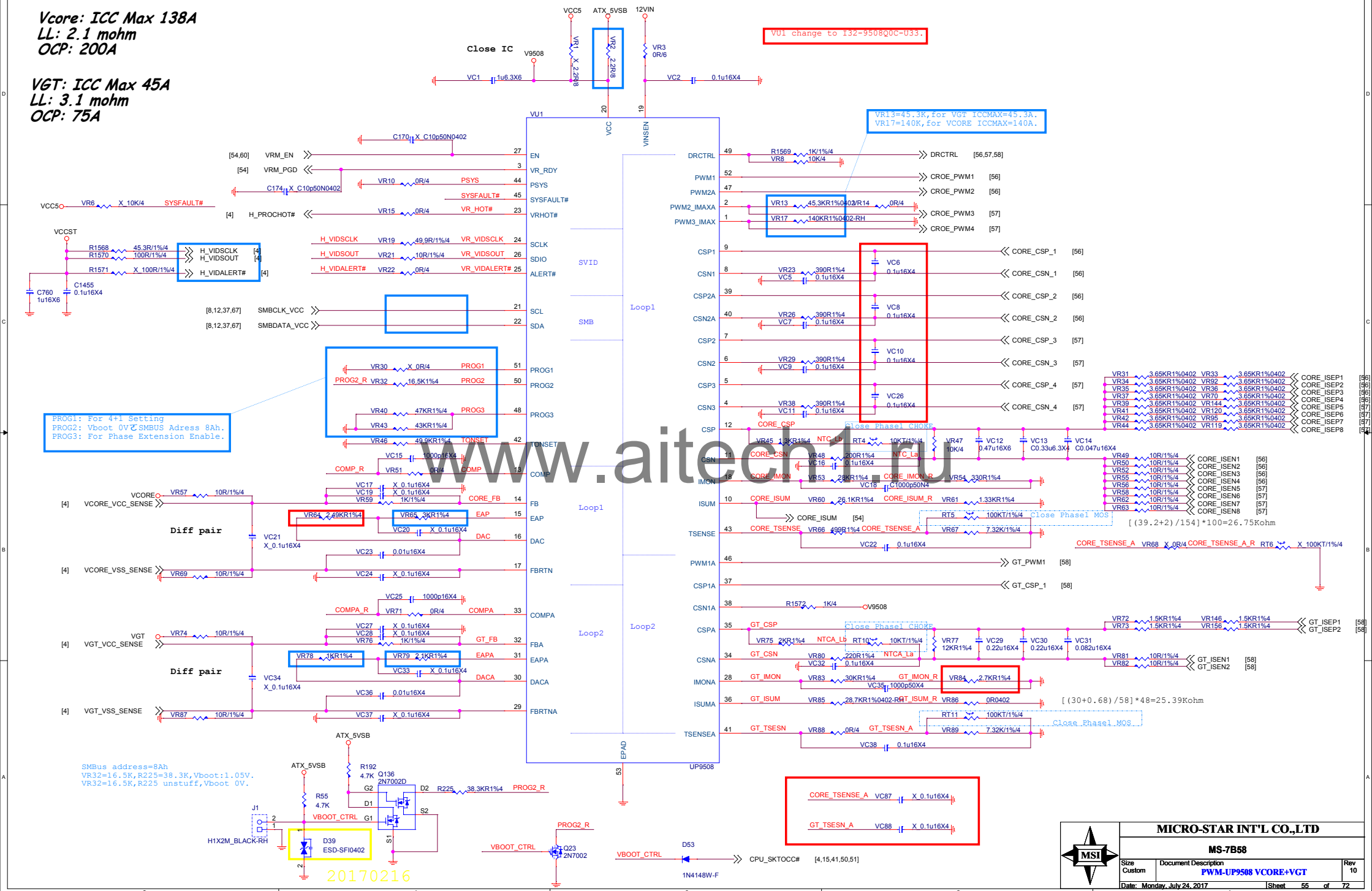
MS-7B58

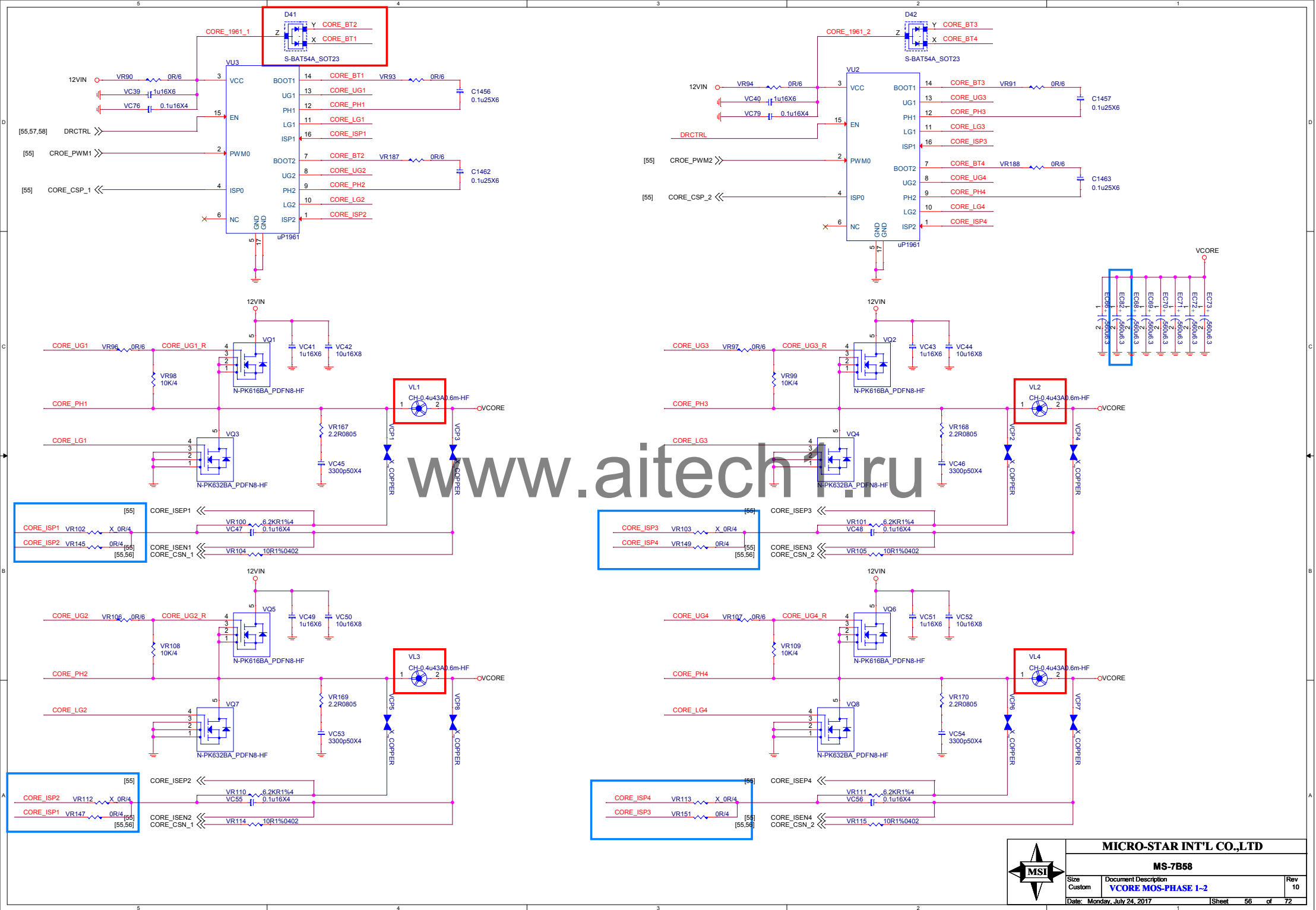
Size Custom	Document Description OV-NCT3933/GPIO-NCT5605	Rev 10
Date: Monday, July 24, 2017		Sheet 53 of 72

PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PG
VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



VGT: ICC Max 45A
LL: 3.1 mohm
OCP: 75A

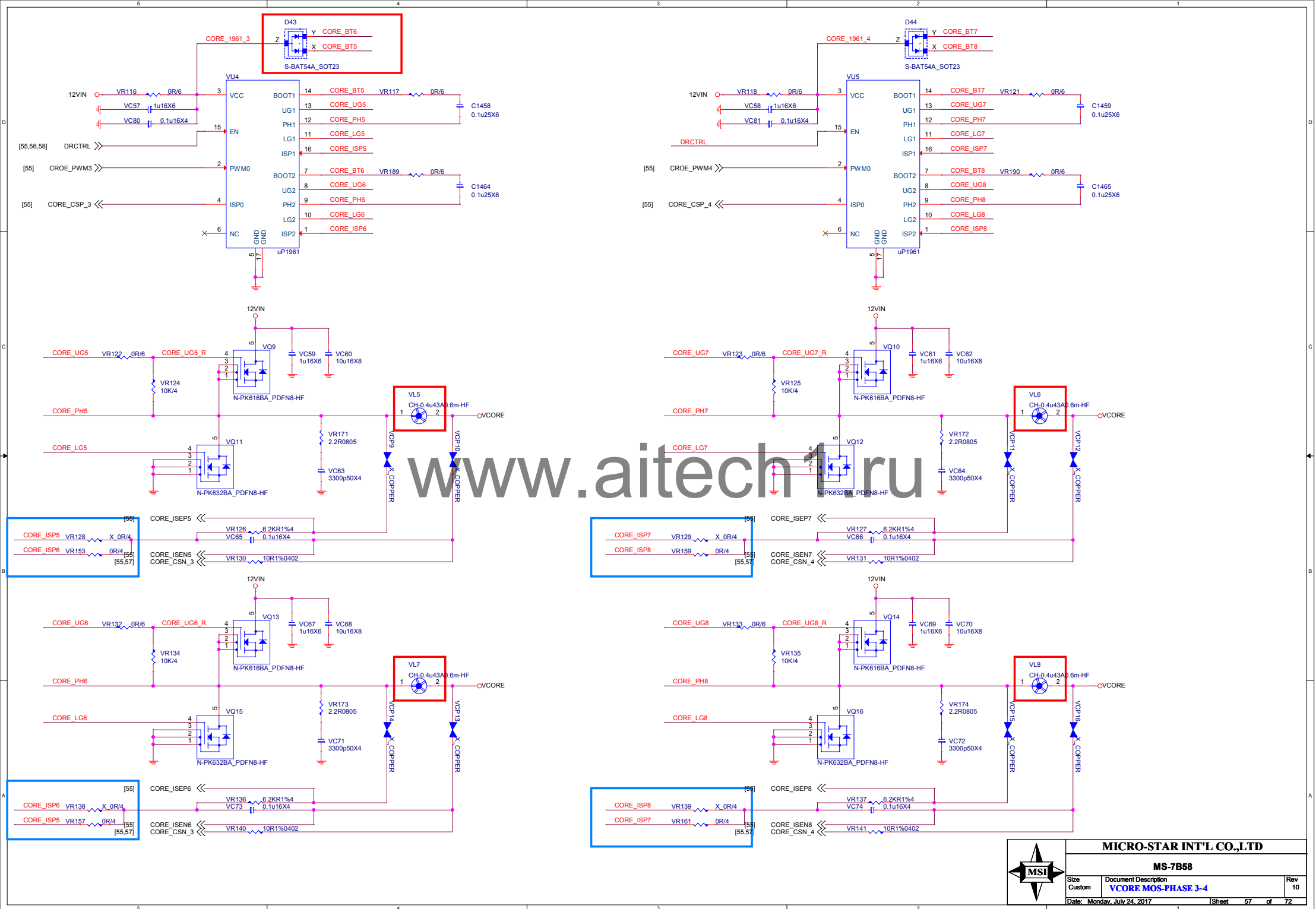




MICRO-STAR INT'L CO.,LTD

MS-7B58

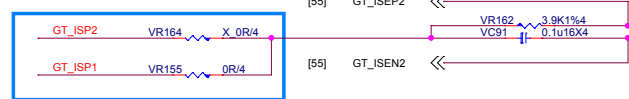
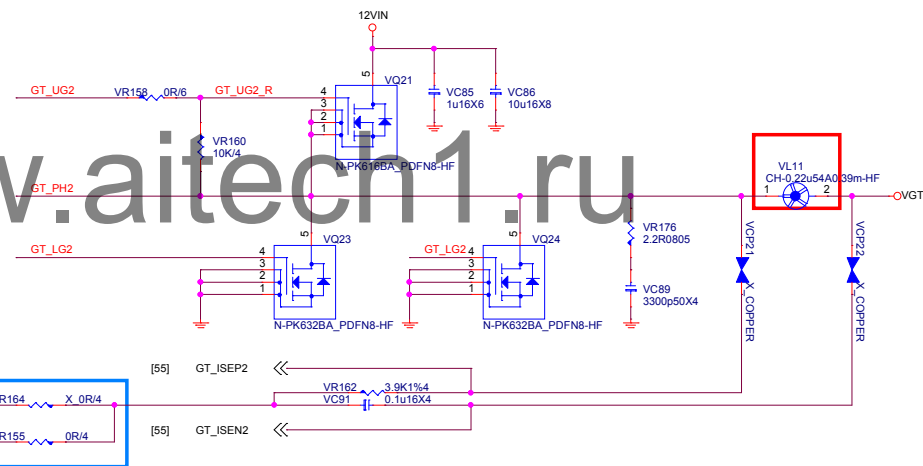
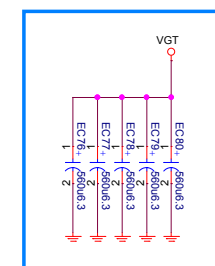
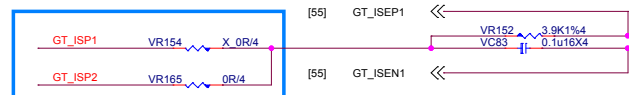
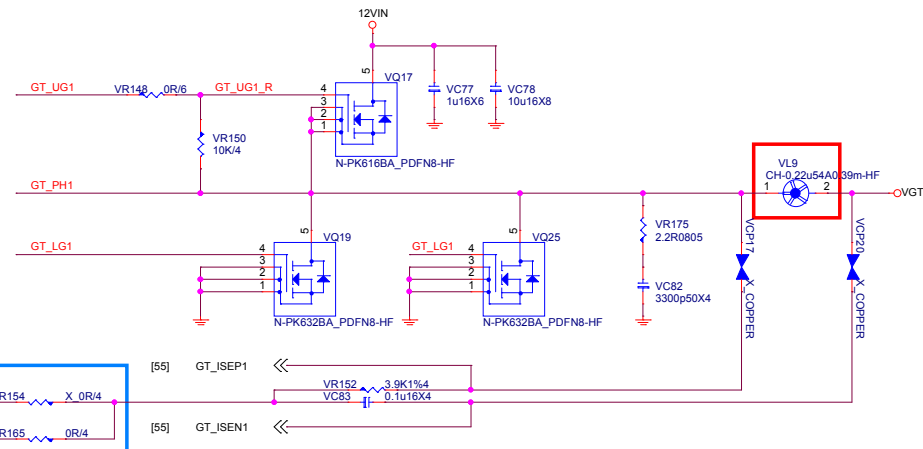
Size	Document Description	Rev
Custom	VCORE MOS-PHASE 1-2	10
Date: Monday, July 24, 2017	Sheet 56 of 72	



MICRO-STAR INT'L CO.,LTD

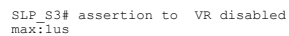
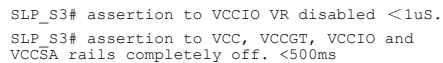
MS-7B58

Size	Document Description	Rev
Custom	VCORE MOS-PHASE 3-4	10
Date: Monday, July 24, 2017	Sheet 57 of 72	



IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685

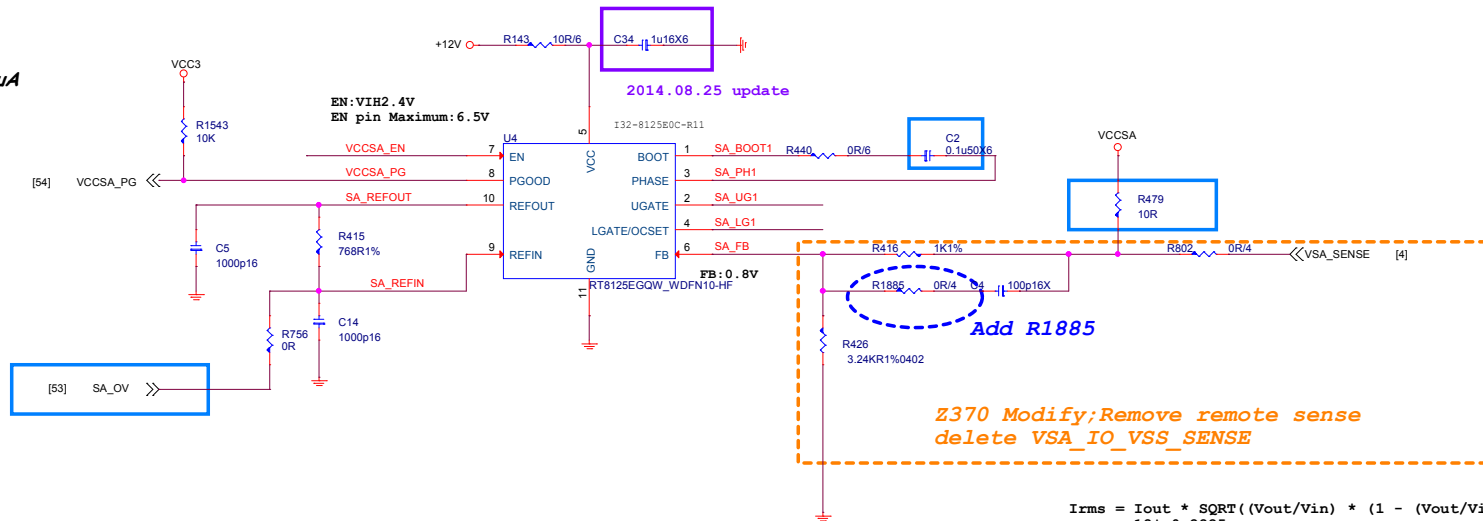


SA Power:1.05V,11.1A

$OCP = 11.1A * 1.4 = 15.54A$
 $R_{ocs}(R417) = OCP * R_{dson}(Low\ side) 3.3m\Omega / 10uA$
 $= 15.54 * (3.3)m\Omega / 10uA$
 $= 5.1282k\Omega$

Rocs: 5.23K, OCP:
D03-632BA0C-N03 : 15.848A

Rdson (Low) 10V
D03-4C05N03-O05 : 3.4mΩ
D03-632BA0C-N03 : 3.3mΩ
D03-3056M00-U47 : 4.2mΩ

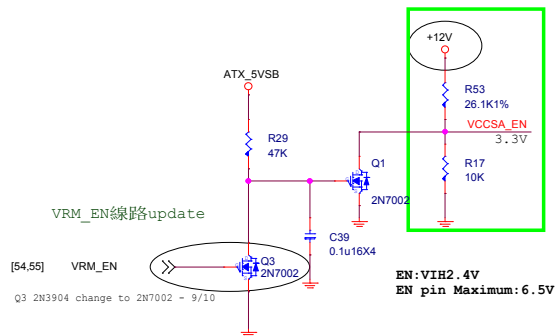


$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 18 * 0.2825$$

$$= 5.086A$$

Pull up by layout & Check level

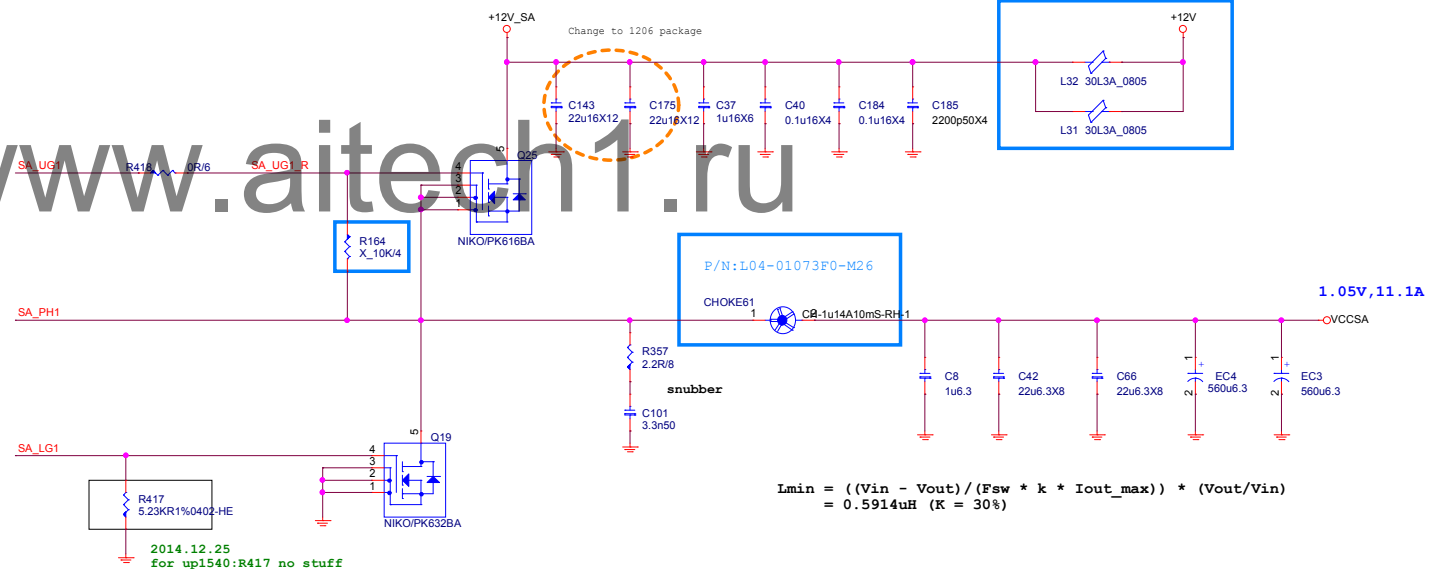


EN: VIH2.4V
EN pin Maximum: 6.5V

[54.55] VRM_EN

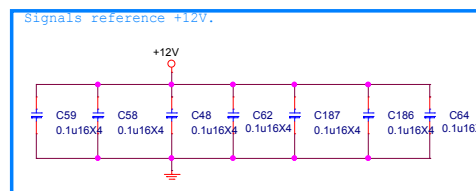
SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled max: 1us



$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.5914uH \quad (K = 30\%)$$



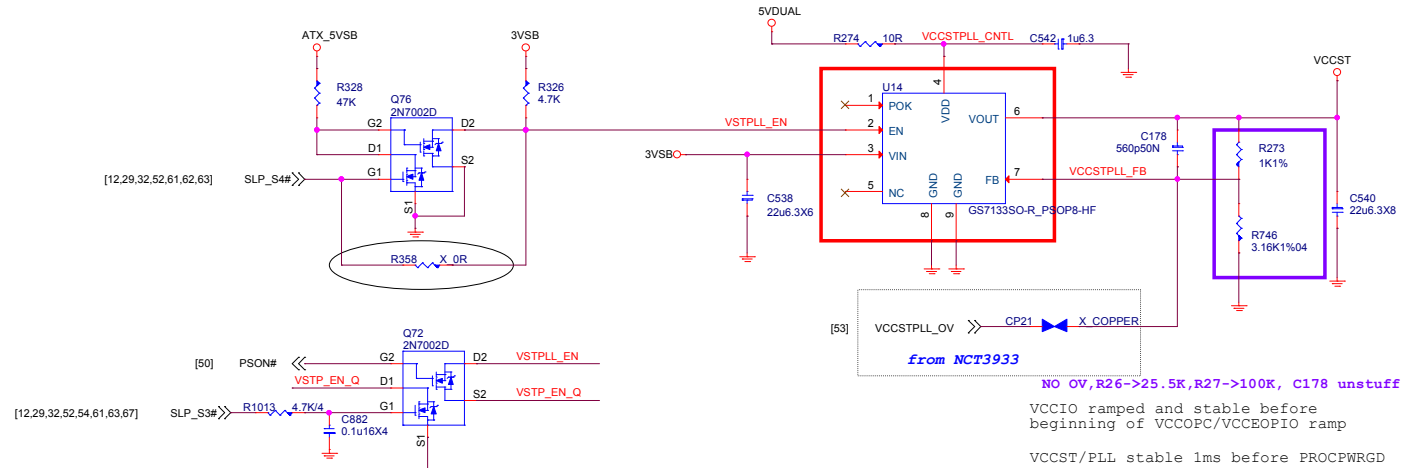
MICRO-STAR INT'L CO.,LTD			
MS-7B58			
Size	Document Description	Rev	
Custom	CPU PWR SA-RT8125C	10	
Date:	Monday, July 24, 2017	Sheet	60 of 72

VCCST

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

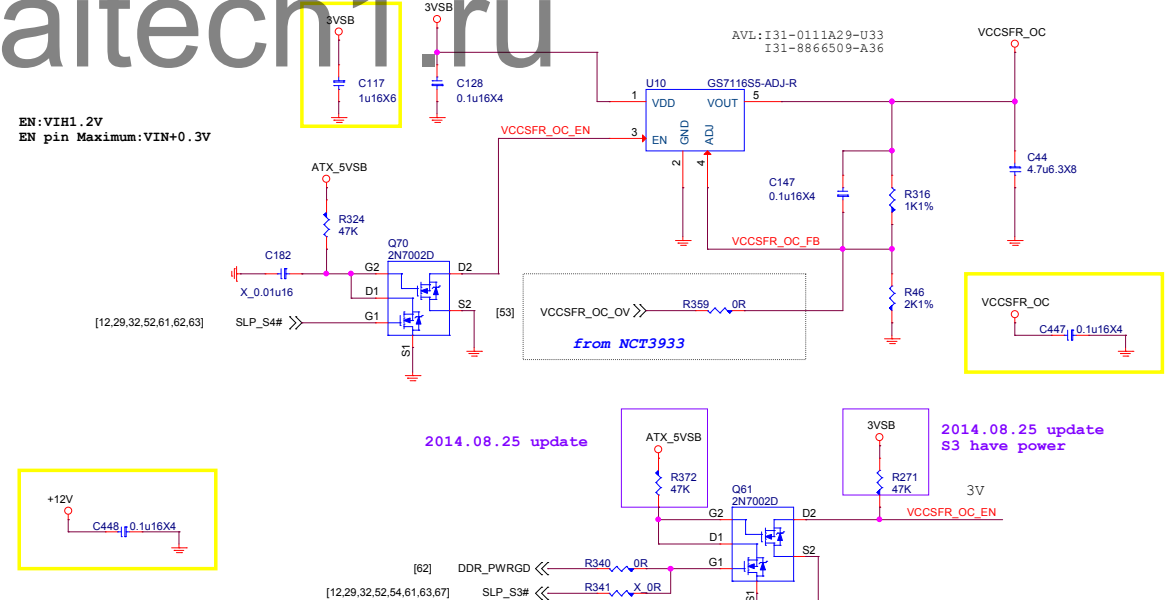
for Gaming3/5, Classic, ECO
and H110



VCCPLL OC

1.2V; 110mA

2014.08.21 update



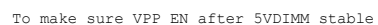
MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	CPU PWR ST/PLL	10
Date:	Monday, July 24, 2017	Sheet 61 of 72

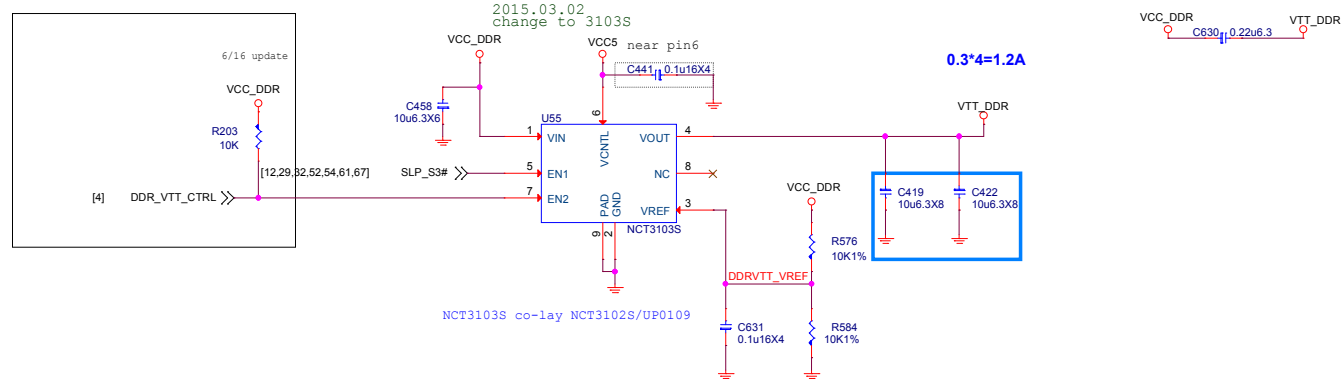


VPP25 Power
2.5V; 2.24A



www.aitech1.ru

2015.03.02
change to 3103S



VCC_DDR VTT_DDR



MS-7B58

Size Custom	Document Description DDR4 Power-VPP25	Rev 10
Date: Monday, July 24, 2017		Sheet 63 of 72

PCH 1VSB

1.0V; 10A(7.929A)

OCP = 15A

Rocset = $1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}$
 = $15A * 4.6m\Omega / 10uA$
 = 6.9K

Rocs: 6.81K, OCP:

D03-632BA0C-N03 : 14.8A

Rdson(LOW) 4.5V

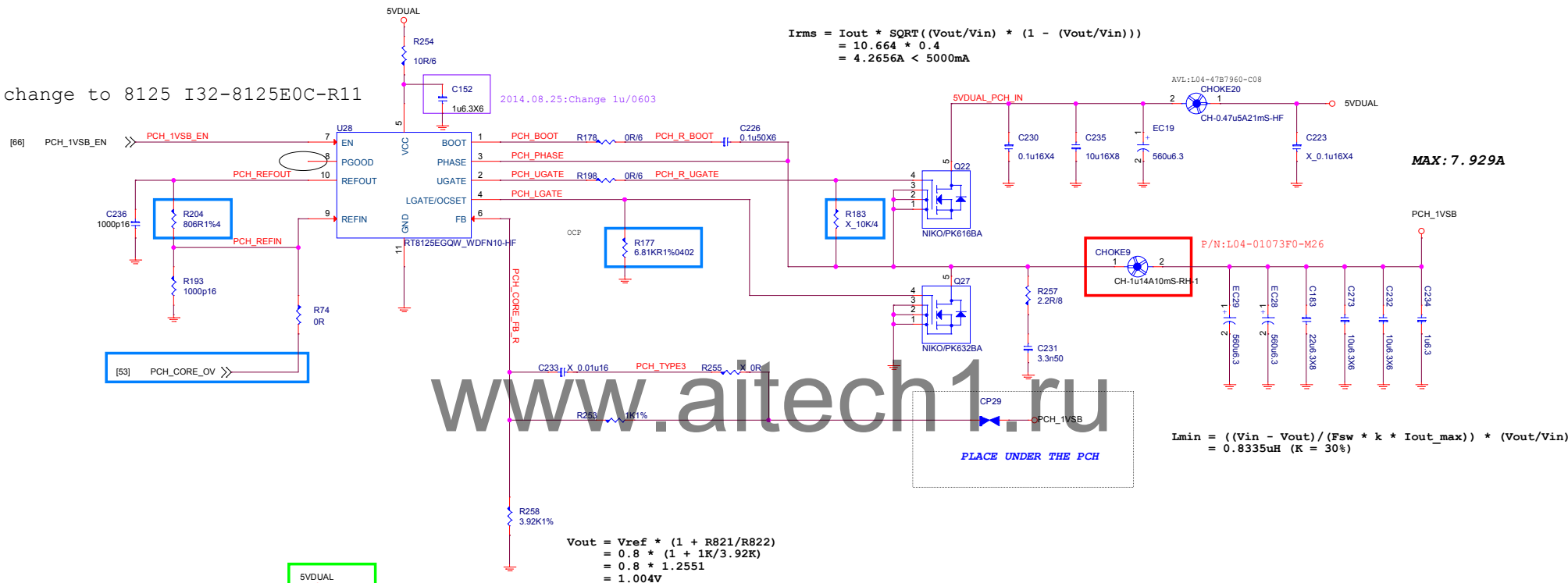
D03-3116M00-U47 : 3.6 mΩ
 D03-632BA0C-N03 : 4.6mΩ
 D03-3056M00-U47 : 6.2mΩ

1504 change to 8125 I32-8125E0C-R11

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$



MAX: 7.929A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

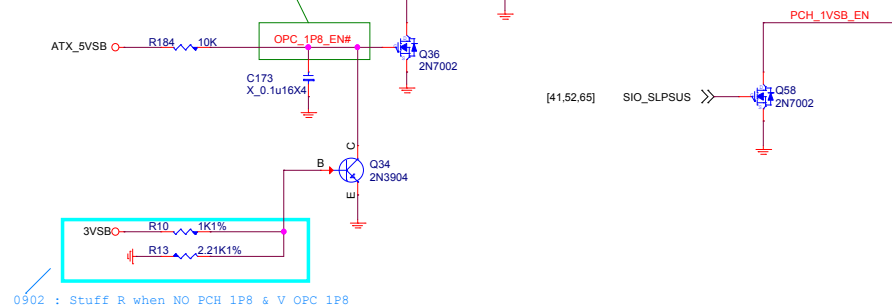
$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$

PLACE UNDER THE PCH

0728: Change net name



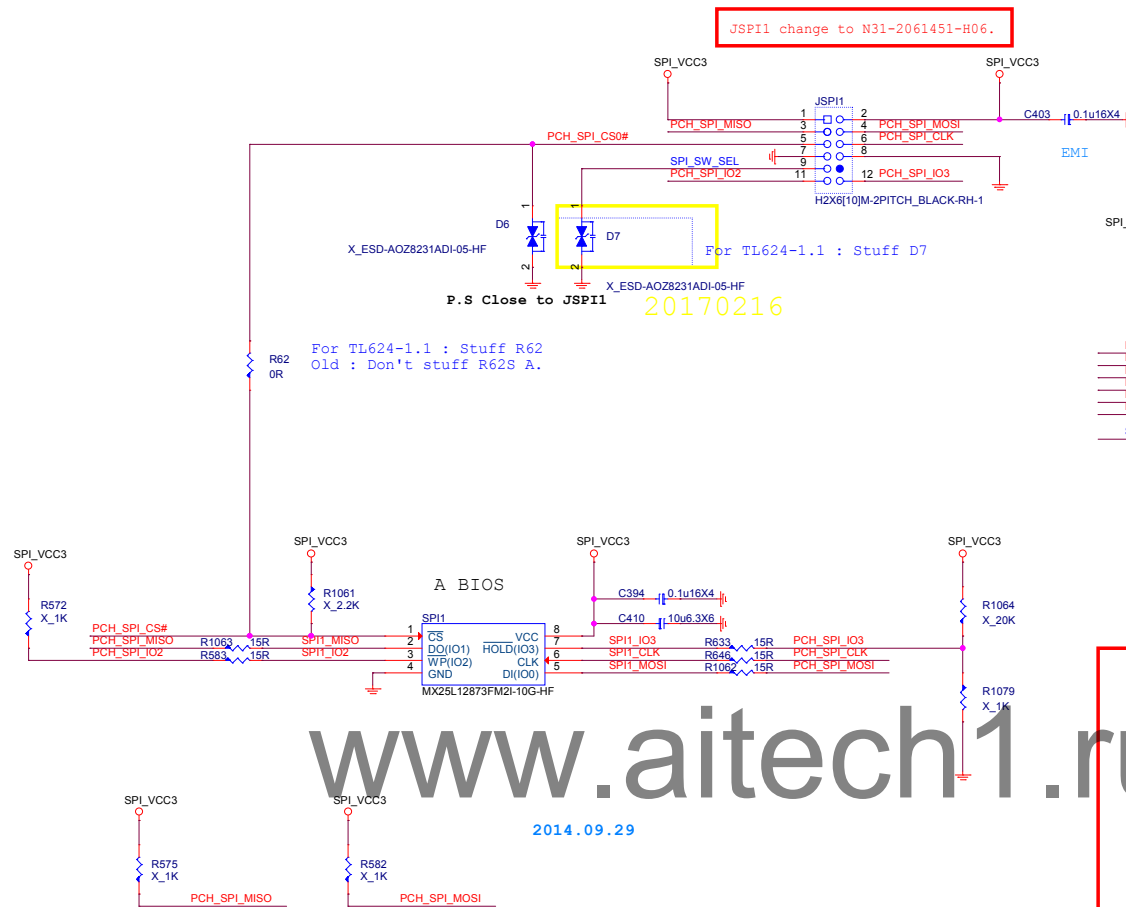
0902 : Stuff R when NO PCH_IP8 & V_OPC_IP8



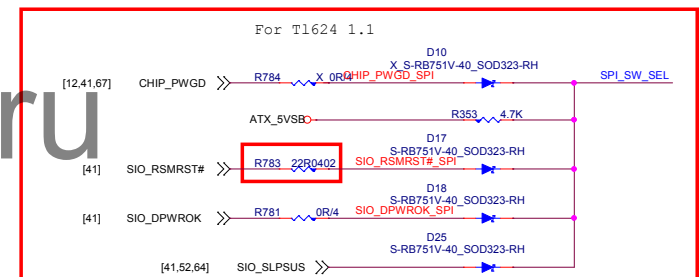
MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	PCH Core Power-RT8125	10
Date: Monday, July 24, 2017	Sheet 64 of 72	



PCH_SPI_CS#	<< PCH_SPI_CS#	[12,32]
PCH_SPI_CLK	<< PCH_SPI_CLK	[12,32]
PCH_SPI_MISO	<< PCH_SPI_MISO	[12,32]
PCH_SPI_MOSI	<< PCH_SPI_MOSI	[12,32]
PCH_SPI_IO2	<< PCH_SPI_IO2	[12]
PCH_SPI_IO3	<< PCH_SPI_IO3	[12]
SPI_SW_SEL	<< SPI_SW_SEL	[32]



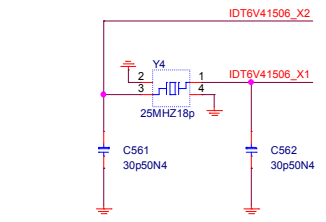
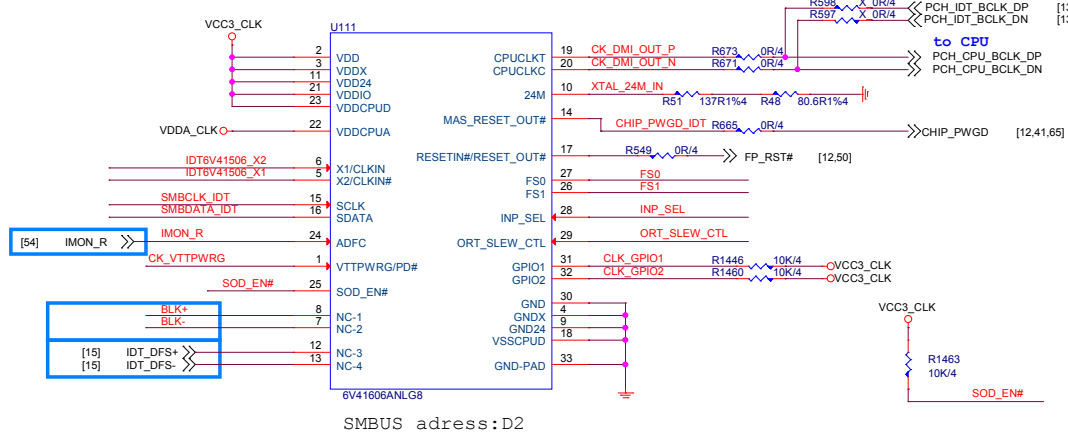
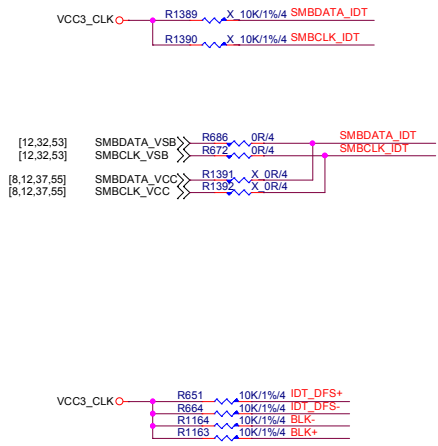
For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272



MICRO-STAR INT'L CO.,LTD

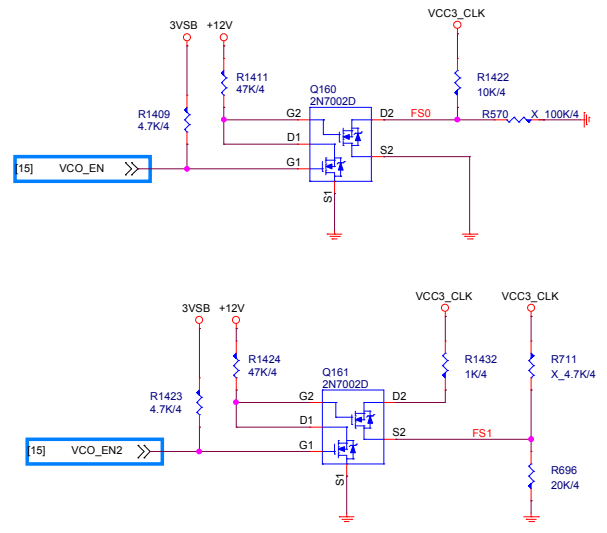
MS-7B58

Size	Document Description	Rev
Custom	BIOS	10
Date: Monday, July 24, 2017	Sheet 65 of 72	



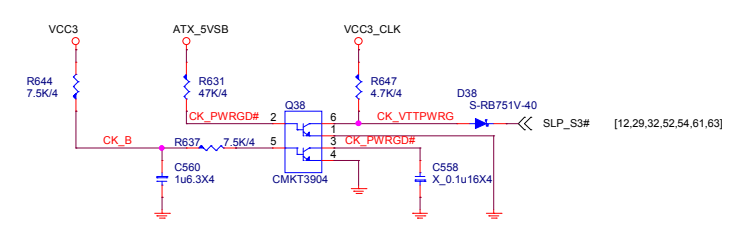
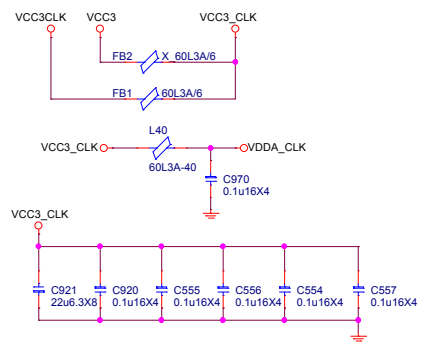
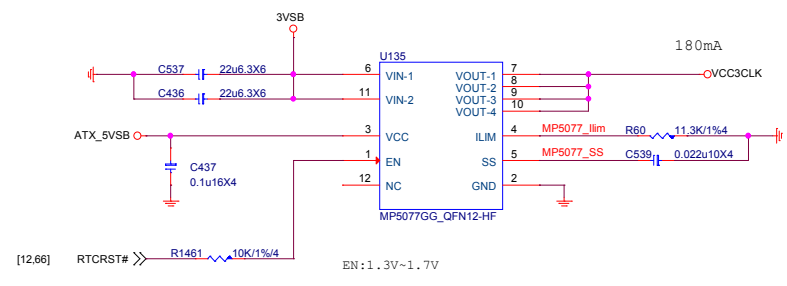
Remove VDDA_CLK OV

www.aitech1.ru



FS1	FS0	VCO Frequency
0	0	VCO 200MHz
0	1	VCO 400MHz (default)
1	0	VCO 1000MHz
1	1	VCO 100MHz

INP_SEL	
0	25MHz crystal input
1	100MHz differential input



MICRO-STAR INT'L CO.,LTD

MS-7B58

Size: Custom

Document Description: CLK Gen- IDT 6V41606A

Date: Monday, July 24, 2017

Rev: 10

Sheet: 67 of 72

PCB



PD0-07A7811-G37
PD0-07A7811-E48

CPU_H1

CPU
鐵座

CPU_H1

BAT1_X1



BAT-BCR2032P-RH

VR Cover



CFOS_LA1

LABEL

CFOS_LABEL

U31_LA1

LABEL

U31_LABEL

BIOS_LA1

LABEL

BIOS_LABEL

HDMI_LA1

LABEL

HDMI_LABEL

NAH_LA1

LABEL

NAH_LABEL

SLI_LA1

LABEL

SLI_LABEL

XSPLIT_LA1

LABEL

SPLIT_LABEL

SSE_LA1

LABEL

SSE_LABEL

MKT_LA1

LABEL

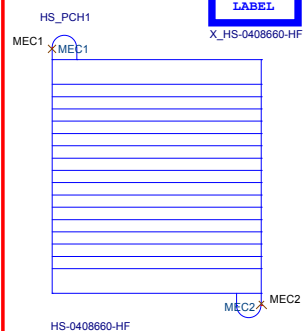
MKT_LABEL

MKT_M6

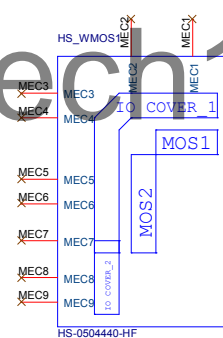
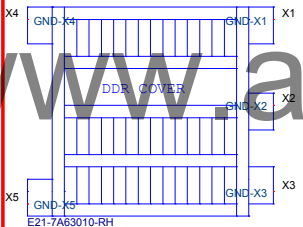
LABEL

X_MKT_LABEL

PCH Heatsink



CV_DDR1

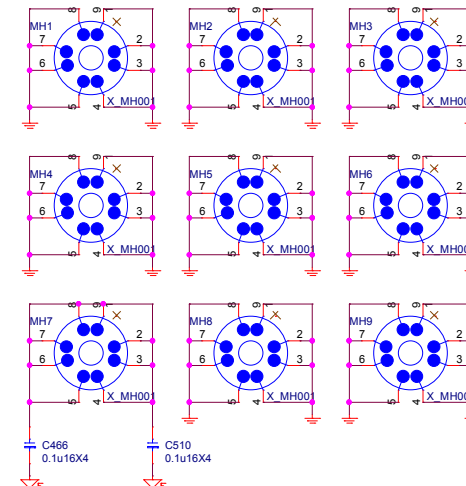


HS_IO_NMOS_M6

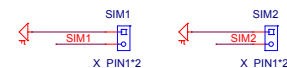
LABEL

HS-0504430-HF

Mounting Holes



Simulation



Optical Fiducial Marks-120

